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Device physics and charge transport of field-effect transistors based on advanced organic semiconductors and graphene

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Device physics and charge transport of field-effect transistors based on advanced organic semiconductors and graphene

by

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Dedication

To my family and God

사랑하는 나의 가족들과 살아계신 주 나의 하나님께 바칩니다.

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Device physics and charge transport of field-effect transistors based on advanced organic semiconductors and graphene

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This dissertation consists of six chapters: In the first chapter, electrical and material properties and charge transport in organic semiconductors and graphene based field-effect transistors (FETs) are introduced. In the second chapter, device architectures of indenofluorene-phenanthrene copolymer based thin-film transistors (TFTs) are discussed. The combination of recessed source/drain and surface treatments on electrical contact and low-voltage-operated TFTs with solution-processed high-k dielectric are investigated. In the third chapter, device physics and charge transport of diketopyrrolopyrrole-naphthalene copolymer based TFTs are discussed. Top-gate TFTs with the polymer dielectric exhibit mobilities of ~1 cm^2/V-s and charge transport measurements in steady-state and under non-quasi-static conditions reveal device physics in dual-gate configuration. In the fourth chapter, device characteristics and charge transport in ambipolar diketopyrrolopyrrole-benzothiadiazole copolymer based TFTs are focused. The ambipolar polymer TFTs possess balanced electron and hole mobilities which are

both > 0.5 cm^2/V-s. The trap density of states is calculated using two analytical methods developed by Lang *et al.* and Kalb and Batlogg. In the fifth chapter, charge transport of diketopyrrolopyrrole-thiophene copolymer based TFTs employing 4-point-probe configuration is studied. Such polymer TFTs possess the mobilities of up to 3 cm^2/V-s. The activation energy as a function of carrier concentration represents multiple trapping and thermally release model or Monroe-type model of charge transport. In the sixth chapter, transformation of electrical characteristics of graphene FETs with an interacting capping layer of fluoropolymers and π-conjugated organic semiconductors is investigated. The electrical properties of graphene by wafer-scale chemical vapor deposition can be favorably tuned by fluorocarbon capping methods.

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CHAPTER 1 INTRODUCTION

1.1 Organic semiconductors

1.1.1 Semiconducting polymers

Most polymers are based on carbon compounds consisting of a repeating structure of unit called a monomer [1-4]. In π- conjugated polymers, delocalization of π-electrons makes the polymer conducting. Since their first discovery has been of great scientific and technological interest [5-6]. They have been investigated for various applications such as large-area, low-temperature, low-cost, and flexible electronics as well as for fundamental research [7-11]. Substantial progresses in high-performance polymeric materials suggest new possibilities for the design of future electronic devices.

In carbon-based polymers with only single bonds, the four atomic orbitals of a carbon atom hybridize and bond with four neighboring atoms with strong σ-bonds. Such polymers are insulating. In the case of π-conjugated or semiconducting polymers, atomic orbits of carbon atoms hybridize in the sp^2 configuration with a p_z orbital accounting for the fourth electron. The sp^2 orbitals form coplanar σ–bonds with a bond angle of 120^o. The p_z orbital which is not involved in the hybridization positions perpendicular to the plane of hybridized sp^2 orbitals. When two atoms bond, the atomic orbitals overlap to form molecular orbitals with lower energy (bonding orbitals) and higher energy (anti-bonding orbitals) compared to the energy of atomic orbitals [12-13]. In most

semiconducting polymers, the electronic properties are determined by π-bonding between the p_z orbitals. The electrons occupy the bonding orbitals. Figure 1.1 shows schematic diagram of the formation of π bonding orbital and π^* anti-bonding orbitals [14].

Since the π orbitals are occupied and the π* orbitals are unoccupied, the highest energy stabilized bonding state is referred to as the highest occupied molecular orbital (HOMO), and the first excited anti-bonding state as the lowest unoccupied molecular orbital (LUMO) [15]. The intermolecular interactions between the HOMO and LUMO in copolymer chain result in further splitting of each molecular orbital to form energy levels and eventually separated HOMO and LUMO bands emerge, as shown in Figure 1.2 [14, 16-17]. HOMO and LUMO correspond in the polymeric semiconductors to the valence band and the conductance band in traditional inorganic semiconductors, respectively. The energy gap (E_g) between the HOMO and LUMO is the energy distance of the primary excitation in organic materials. Many of the material and electrical properties of organic/polymeric semiconductors result from the energy level of HOMO and LUMO and the energy gap between HOMO and LUMO as well as the electronic overlap between molecules which is essential for charge transfer and transport.

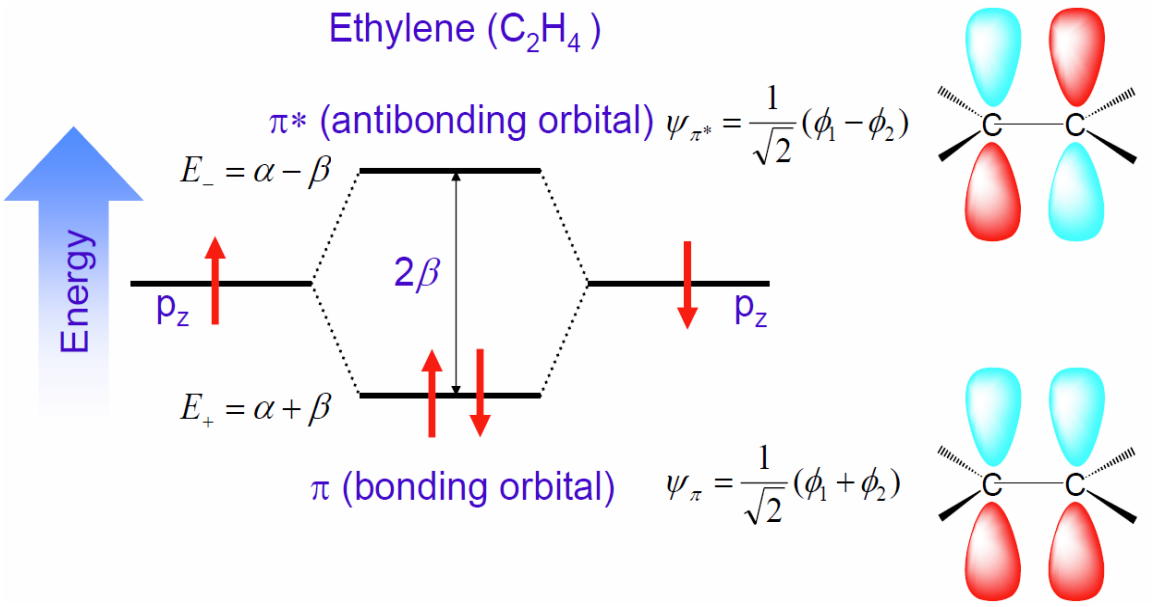


Figure 1.1 Schematic diagram of formation of π bond orbital and π^* anti-bonding [From 14]

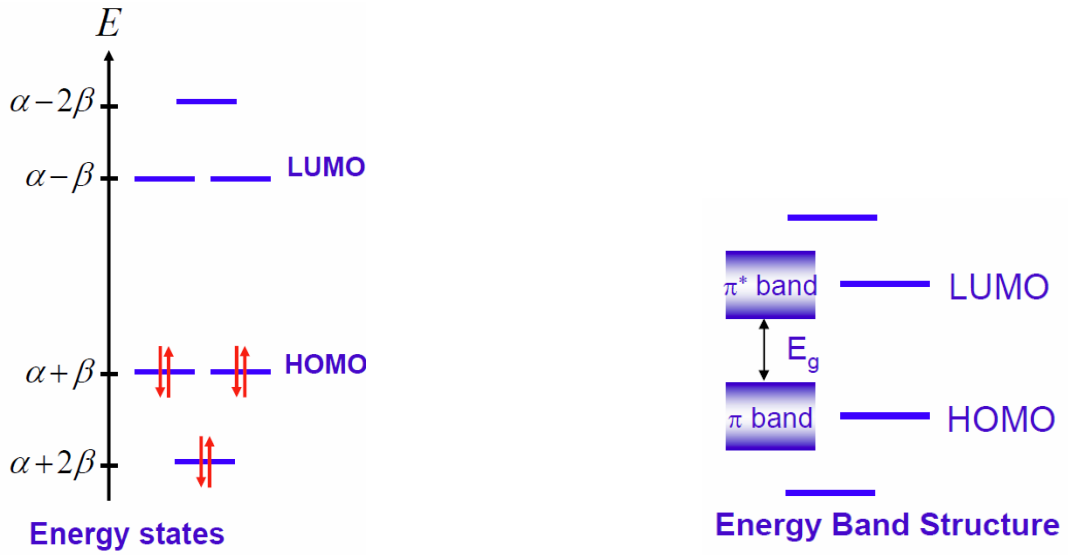


Figure 1.2 Illustration of energy states and band formations [From 14]

1.1.2 Charge transport in organic/polymeric semiconductors

Polaron

Compared to most conventional inorganic semiconductors with adequately high mobility, in which charge transport occurs through band transport, charge carriers in most organic semiconductors move by hopping. This is because the molecules are bound by weak van der Waal's forces rather than strong covalent bonds. Strong carrier-phonon interaction leads to charge localization by polaron formation [18-19]. A polaron is a quasiparticle representing the combination of the charge carrier and the corresponding lattice distortion [19]. In other words, localization in conjugated organic semiconductors occurs through the formation of polarons. This localization is in most cases compounded by defects and impurities which produce trap states in the energy gap. In the absence of a significant concentration of defects (for example, in certain purified molecular crystals such as rubrene), band transport can take place at lower temperatures where the electronic bandwidth exceeds the polaron binding energy. Such delocalized transport is also expected in conjugated polymers, in which the electronic bandwidths are often higher than in molecular crystals. However, defects and domain boundaries have prevented the clear observation of delocalized transport in conjugated polymers. Nevertheless, evidence of delocalization of charge carriers in polymers has been reported [20].

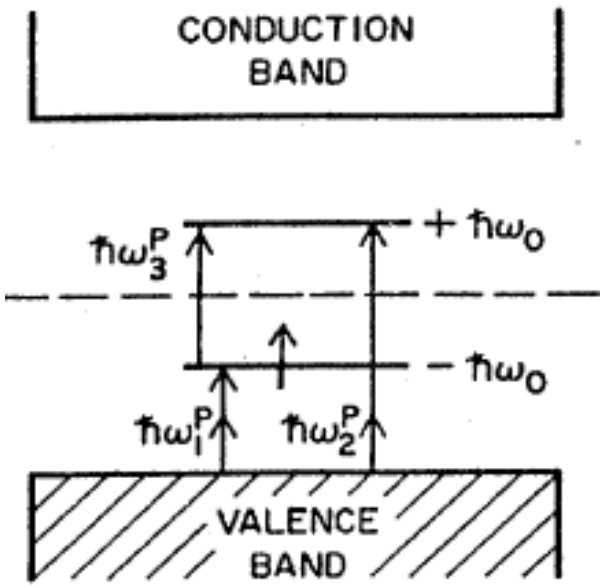


Figure 1.3 Band diagrams of polaron with the localized gap states [From 19]

Hopping (Phonon-assisted quantum mechanical tunneling)

In most organic semiconductors, charges move through a series of localized states. Hopping is one of the possible mechanisms of charge transport and is clearly observed in amorphous and disordered organic semiconductor [21-24]. Hopping can be modeled by means of the Miller-Abrahams hopping rate equation as shown below [25-26]:

$$\omega_{ij} = \gamma \begin{cases} \exp\left[-\left(-2\alpha + \dfrac{qE}{k_B T}\cos\theta\right)R_{ij} - \dfrac{\varepsilon_j - \varepsilon_i}{k_B T}\right], & \varepsilon_j - \varepsilon_i \geq qER_{ij}\cos\theta \\ \exp(-2\alpha R_{ij}) & \varepsilon_j - \varepsilon_i \leq qER_{ij}\cos\theta \end{cases}$$

where ε_i and ε_j are the energy in the absence of electric field at one site, i and another site, j, γ depends on the phonons spectrum, α-1 is the Bohr radius of the localized wave function, k_B is the Boltzmann constant, q is the electrons charge, R_{ij} is the distance between the two sites i and j, and θ is the angle between F and R_{ij}. The transition rate of a carrier hopping from i to j is given by ω_{ij} as shown above. When the temperature increases, the transition rate becomes larger.

The localized states are distributed with a Gaussian density of states [26]. There are various transport models which either take into account or ignore correlations between the energies of adjacent states [21, 23, 26]. The charge carriers hop between the states either upward or downward in the energy states as well as hop a short distance with high activation energy or a long distance with low activation energy. The charge carriers tend to hop to a larger distance rather than to the nearest neighbors to occupy a more favorable energy state. This process is the so-called variable range hopping mechanism and was first described by Mott [27-29]. According to the Mott's approach, the conductivity can be extracted from following equation [29]:

$$\sigma = \sigma_0(T)\exp[-(T_o/T)^{1/4}]$$

where σ is conductivity and T is a temperature.

If the Coulomb gap can be not neglected through Coulomb interaction, the conductivity is extracted by means of a slightly different equation reported by A. L. Efros and B. I. Shklovskii [30]:

$$\sigma = \sigma_0(T)\exp[-(T_o/T)^{1/2}]$$

Multiple trapping and thermally release

Multiple trapping and release (MTR) model has been used to explain charge transport in amorphous silicon which has a narrow delocalized band and large activation energy associated with a high concentration of localized levels [31]. While charge carriers move through the quasi-delocalized levels, they interact with the localized states through trapping and thermal release [32]. The basic MTR model was modified by Monroe for systems in which transport is dominated by hopping within the band tail in addition to thermal excitation to the band edge [33]. This model is more applicable to organic semiconductors where polaronic effects and disorder effects make band-like transport difficult to achieve even in pure crystalline materials.

If the field-effect mobility in devices is plotted as a function of the inverse of temperature, an Arrhenius relation is obtained with the activation energy E_a [34]

$$\mu_{FET} = \mu_0 \exp\left(\frac{-E_a}{kT}\right)$$

where k is the Boltzmann constant, T is a temperature, E_A is activation energy and μ is field-effect mobility. The activation energy roughly corresponds to the energy distance between occupied trap states and the transport level.

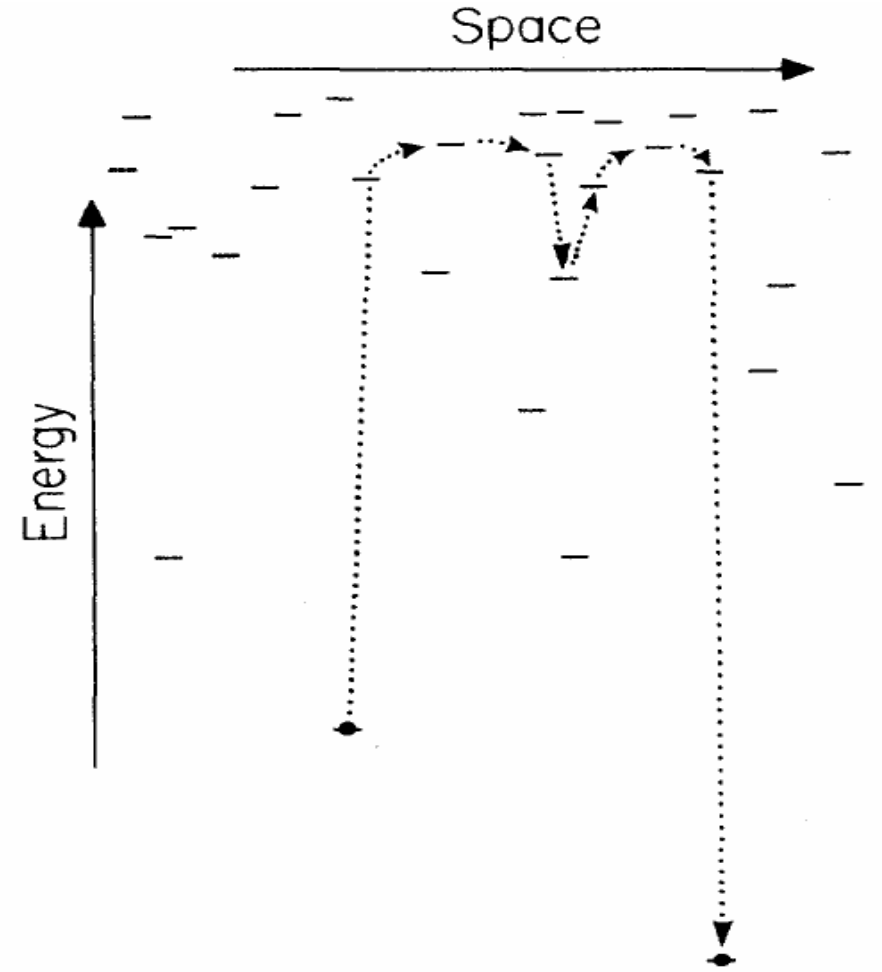


Figure 1.4 Illustration of Monroe model of charge transport [From 33]

1.2 Organic field-effect transistors

1.2.1 Device configurations

In principle, organic/polymeric semiconductors can transport both charge carriers, but one type of charge carrier frequently becomes trapped in states present at the interface between the semiconductor and the dielectric layer and in the gate insulator on organic

field-effect transistors (OFETs) [32]. Figure 1.5 shows the energy band diagrams of prototypical unipolar and ambioplar operation in transistors along with their expected electrical characteristics [35]. For $V_G > V_{SD}$, the electrons are injected from the source and the charge density profile characteristic of a FET operating in the linear region. However, for $V_{SD} > V_G$, holes can be injected at the drain and a situation where electrons and holes are injected simultaneously from both source and drain electrodes can happen as shown in Figure 1.5.

At low negative gate voltages in the hole-enhancement mode, the drain current increases with decreasing gate voltage and does not saturate but instead increases non-linearly with drain voltage. This is a result of electron injection from the drain. Similarly, at low positive gate voltage in the electron-enhancement mode, a non-saturating current with increasing drain voltage and decreasing gate voltage is observed. This is due to hole injection from the drain. At higher gate voltages, linear and saturation regions, expected for a field-effect transistor operation in accumulation mode, are clearly observed.

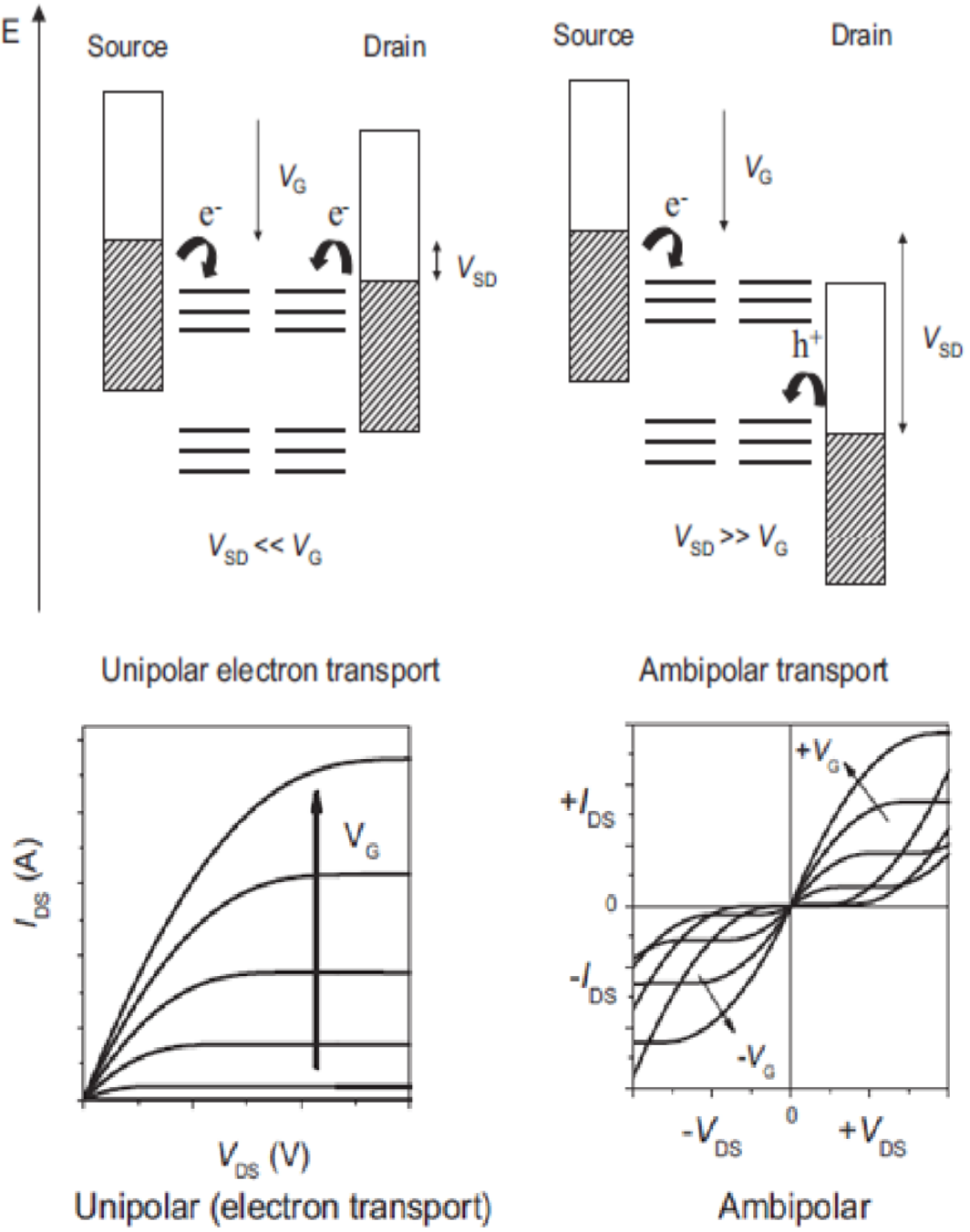
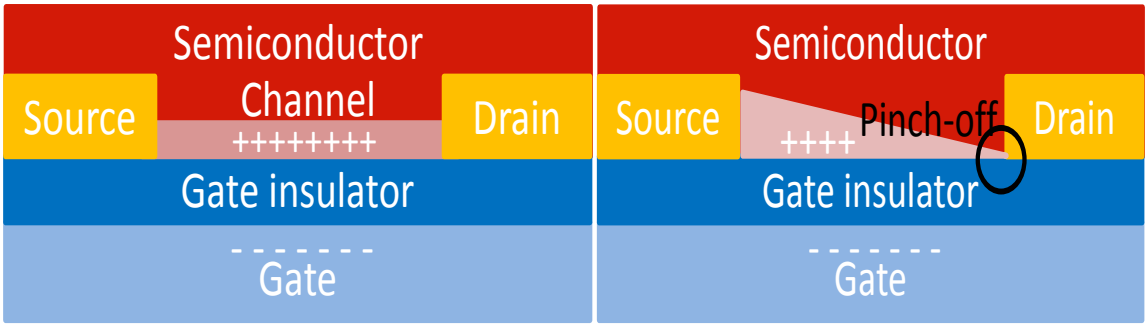


Figure 1.5 Energy band diagrams of unipolar and ambioplar operation in devices along with their expected electrical characteristics [From 35]

1.2.2 Unipolar device operation

Figure 1.7 shows schematic cross sections of OFET in the linear and saturation operation modes. The basic device structure of OFETs consists of three electrodes (source, drain and gate), gate dielectric (gate insulator) and active semiconductor layers [36-37]. The source and drain electrodes inject the charge carriers to the semiconductor and collect the charge carriers from the semiconductor. The gate electrode is isolated from the active semiconductor layer by a gate dielectric layer and serves to form a field-induced charge distribution in the semiconductor. Beyond a certain gate voltage, majority charge carriers are accumulated at the interface between gate insulator and semiconductor layers, which forms a conducting path, called a channel.



(a) (b)

Figure 1.6 Schematic cross section of OFETs with different operation modes: (a) linear region and (b) saturation region

In the linear region ($|V_{DS}| < |V_G - V_T|$), the distribution of accumulated charge density in the channel region is uniform. The drain current I_D is given by [37]

$$I_D = \frac{W\mu_{lin.}C_i}{L} \times \left((V_G - V_T)V_{DS} - \frac{V_{DS}^{\ 2}}{2} \right)$$

where W, L, C_i, V_G, and V_T represent the channel width, the channel length, the capacitance of the gate dielectric per unit area, the gate voltage, and the threshold voltage, respectively.

As the drain-source voltage increases, the distribution of charge carriers near the drain electrode is changed and eventually the channel is pinched-off. In the saturation region ($|V_{DS}| \geq |V_G - V_T|$), the drain current I_{DS} is given by [37]

$$I_{DS} = \frac{W\mu_{sat.}C_i}{2L} \times (V_G - V_T)^2$$

The mobility at each operating point can be calculated using the transconductance $\partial I_D/\partial V_G$ from experimentally obtained transfer curves.

1.3 Graphene

1.3.1 Carbon compounds

Figure 1.8 shows the allotropes of carbon from 0-dimensional to 3-dimensional structures [38]. One example of a 0D allotrope is C_{60} which has a soccer ball shape and consist of 60 carbon atoms, 1D forms include carbon nanotubes (CNTs), the 2D form is designated graphene and 3D forms include diamond (net structure) and graphite (sheet structure). As shown in Figure 1.9, it is possible to generate many of these allotropes from a sheet of graphene [39].

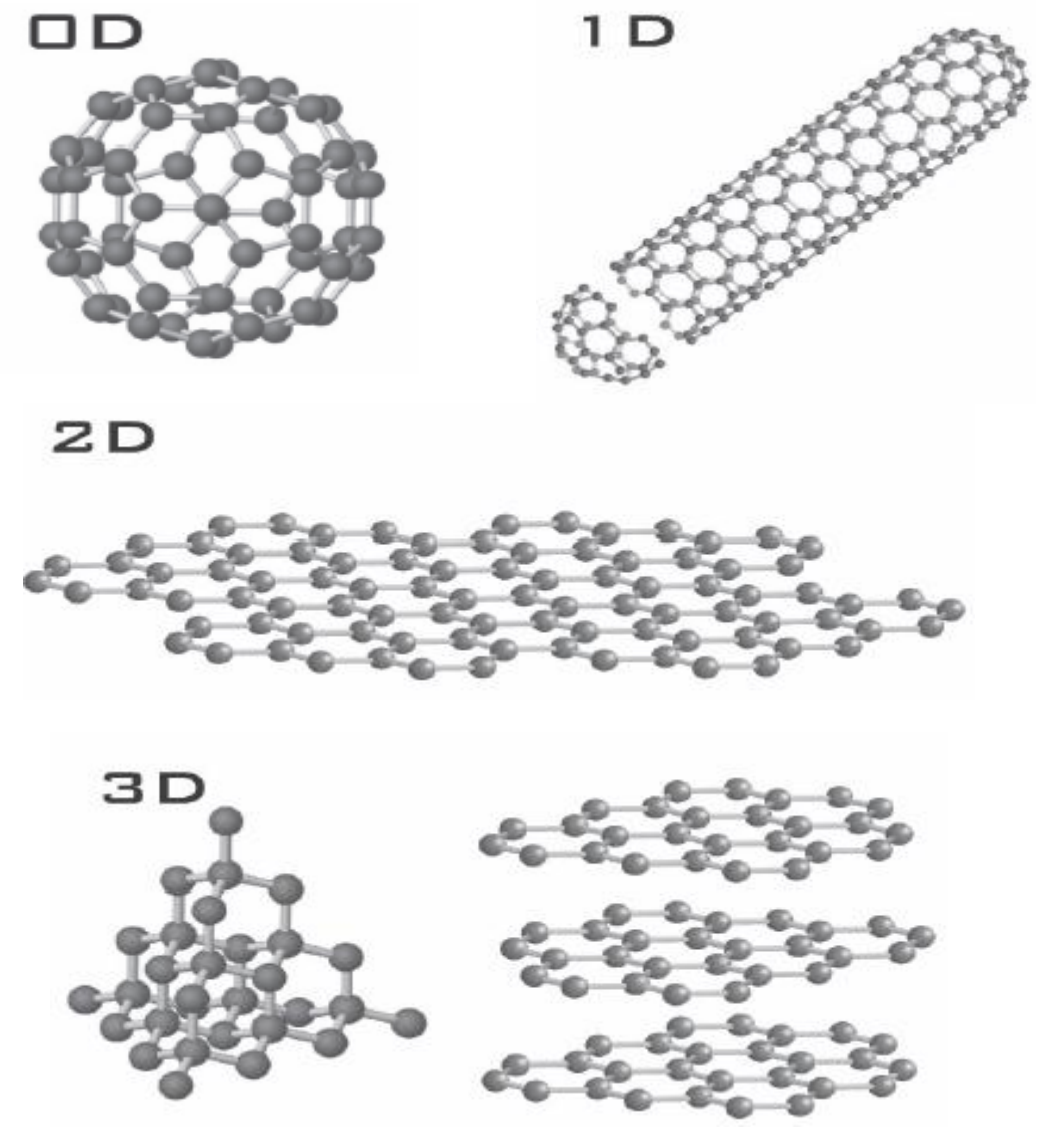


Figure 1.7 The allotropes of carbon from 0 dimensional to 3 dimensional structures [From 38]

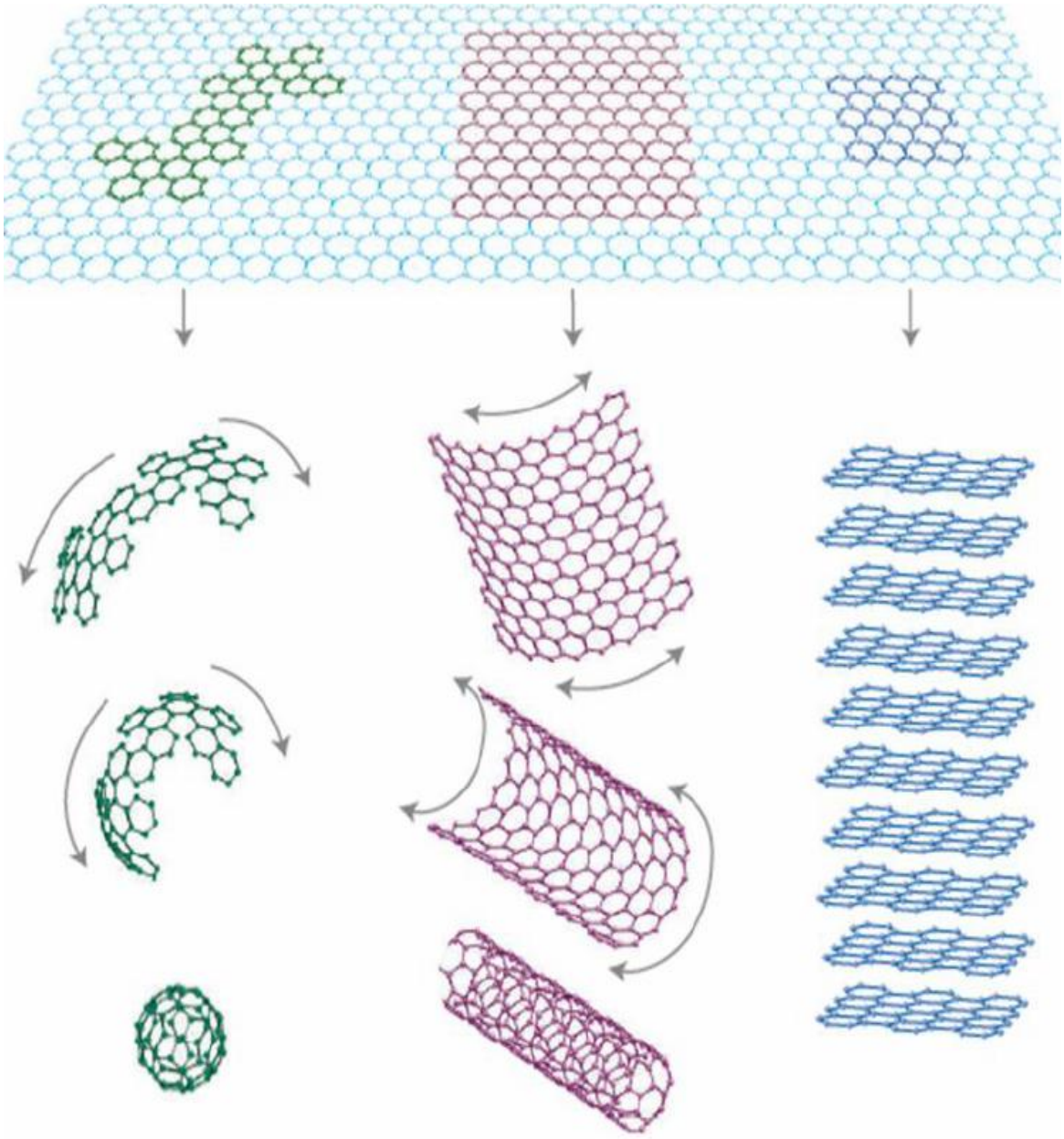
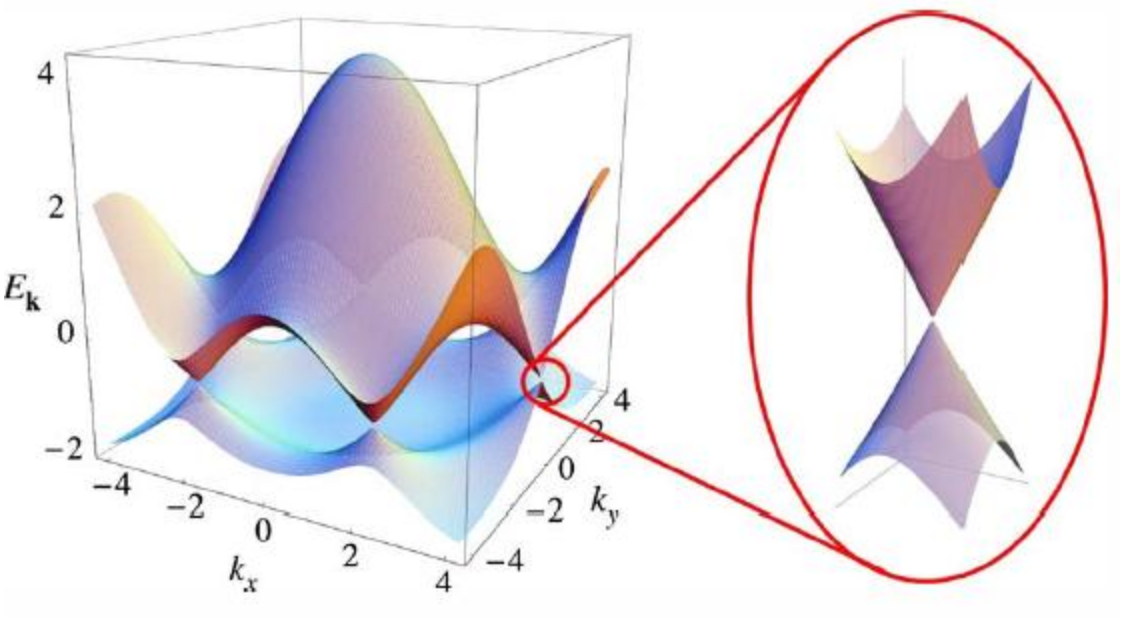


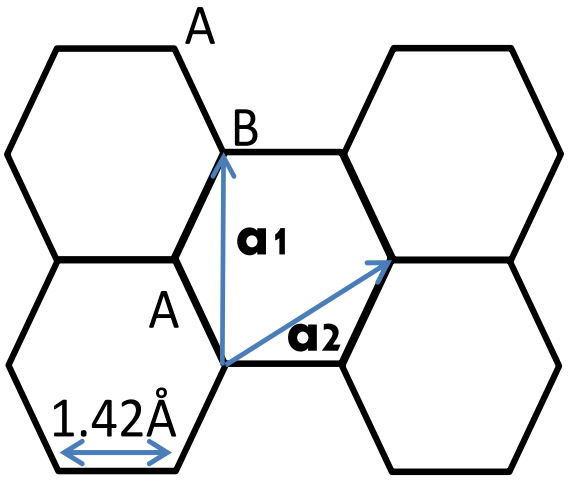
Figure 1.8 The illustration of how to make different dimensional forms from graphene [From 39]

1.3.2 Electronic structure of graphene

Graphene (defined as being a single layer of graphite) is a two-dimensional hexagonal lattice consisting of carbon atoms [39-40]. Each carbon atom is covalently bonded with nearest neighbors through sp^2 hybridization. The π bands are well-characterized as linear combinations of p orbitals of the carbon atoms [41]. The unit cell is based on two carbon atoms (two nonequivalent sub-lattices, A and B) and the carbon-carbon bond length is 1.42 Å [41]. Hopping transport between the sub-lattices results in the formation of two energy bands, and the structure is established with two conical points per Brillouin zone where band crossing occurs at the K and K' points. These points are called Dirac point as shown in Figure 1.9 [40]. The band structure of graphene as shown in Figure 1.9, indicates that the conduction band and the valence band intersect at the Dirac point and the electron energy is linearly dependent on the wave vector. As a result, quasiparticles in graphene exhibit a linear dispersion relation $E = \hbar k \upsilon_F$, as if they are massless relativistic particles [42-43]. In graphene, the charge carriers mimic particles, which are governed by the Dirac equation rather than the Schrödinger equation which is commonly employed in the analysis of conventional solid state systems where effective mass corresponds to the curvature of the band structure [43]. Based on the band-structure, intrinsic graphene is a semi-metal or zero-gap semiconductor [44].



(a)



(b)

Figure 1.9 (a) Band structure of graphene [From 40] and (b) sub-lattices structure

1.3.3 Electronic properties of graphene

It was reported that the electron mobility at room temperature in exfoliated graphene is excess of 15000 cm^2/V-s at a carrier concentration of 10^{12} cm^{-2} [45]. In addition, suspended graphene exhibits the mobility of up to 200000 cm^2/V-s with carrier

concentration of $2x10^{11}$ cm^{-2} at room temperature [46]. However, since scattering of electrons by optical phonons from the substrate dominates at room temperature, device performance is limited in graphene FETs [47-48]. Furthermore, impurities that incorporate into the film during the fabrication process also become a scattering source. Recently, boron-nitride (BN) has been used as a substrate for the graphene since BN possesses a high phonon energy and does not incorporate impurities due to the absence of out-of-plane bonds [49-50]. Figure 1.10 shows the scattering mechanisms in graphene [51]. Whereas surface optical phonon scattering is dominant at lower electron energy, optical phonon scattering limits the mobility at higher electron energy.

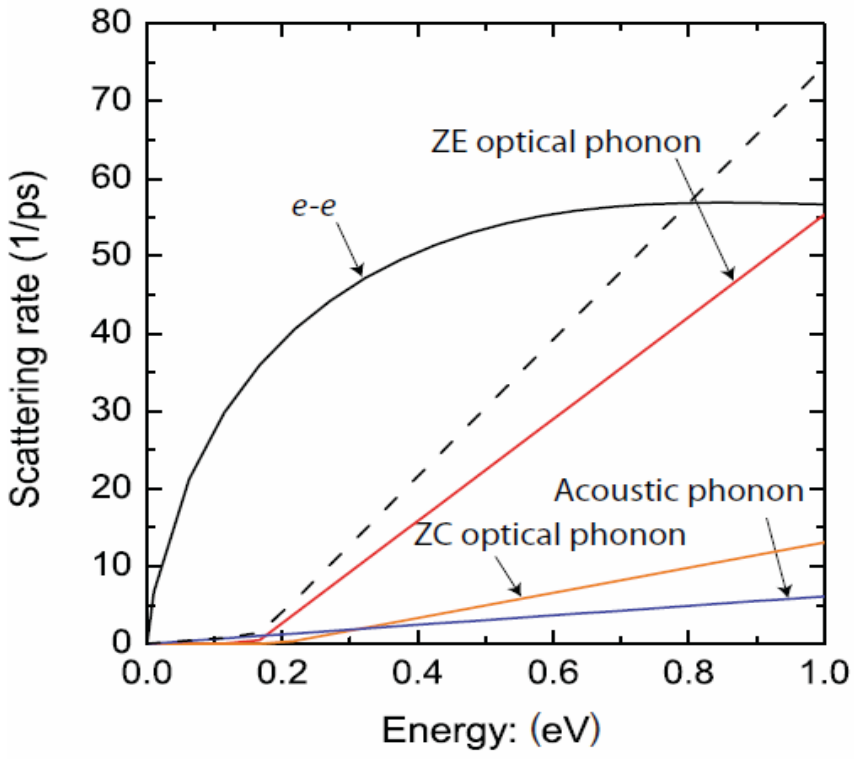


Figure 1.10 Scattering rates vs. energy in graphene [From 51]

In addition, since graphene has a zero band-gap, FET devices possess high off-currents, making it difficult to use them as logic devices, which require on-off current ratios in excess of 10^4-10^6 [52]. Graphene must have a band-gap energy of at least 0.4 eV to be useful in logic device applications [52]. Instead of applications that demand a large on-off current ratio, graphene FETs are expected to be useful in radio frequency (RF) applications. There have been previous attempts to improve the on-off current ratio in graphene FETs [53-54]. In addition, graphene FETs with a 100 GHz cut-off frequency have been achieved, which is a remarkable result since it is higher than what silcon FETs have been able to achieve [55]. However, absence of current saturation in the output characteristics of graphene is not ideal for RF device performance.

1.3.4 Charge transport in graphene

1) Diffusive transport

Chen et al. and Hwang et al. reported that the transport in graphene is affected by charged impurities which act as scattering centers through long range Coulomb scattering [56-57]. Figure 1.11 shows graphene conductivity limited by Coulomb scattering. The linear relation between conductivity and carrier concentration is observed.

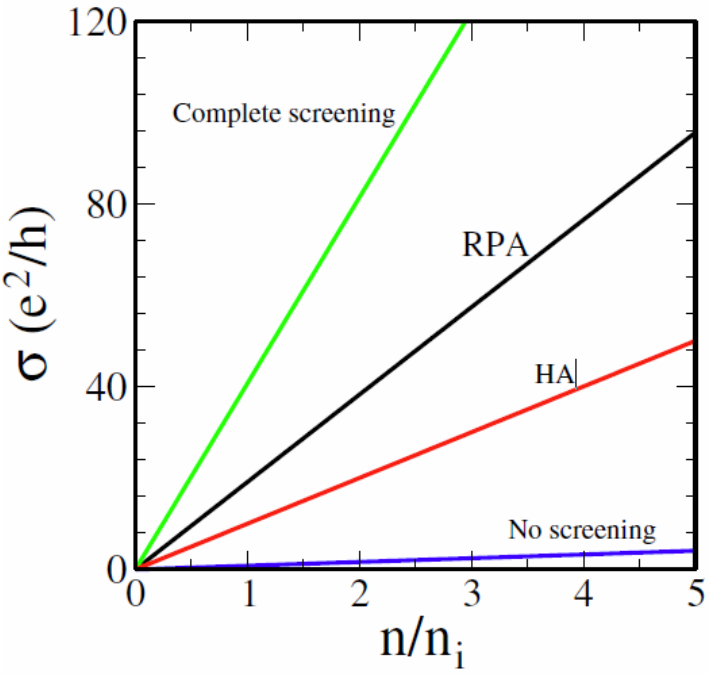


Figure 1.11 Graphene conductivity as a function of carrier density with random phase approximation (RPA) and Hubbard approximation (HA) screens [From 57]

2) Self-consistent theory

The charged impurities present random voltage fluctuations in the graphene layer, which leads to a shift in the Dirac point and induces a residual carrier density due to electron and hole puddle formation caused by the charged impurities [58]. The charged impurities act as scattering centers and also reduce the mobility. Figure 1.12 shows the results of self-consistent calculations [58]. The results indicate that the graphene minimum conductivity is not universal and the shift in Dirac point is related with the residual carrier density induced by potential fluctuation.

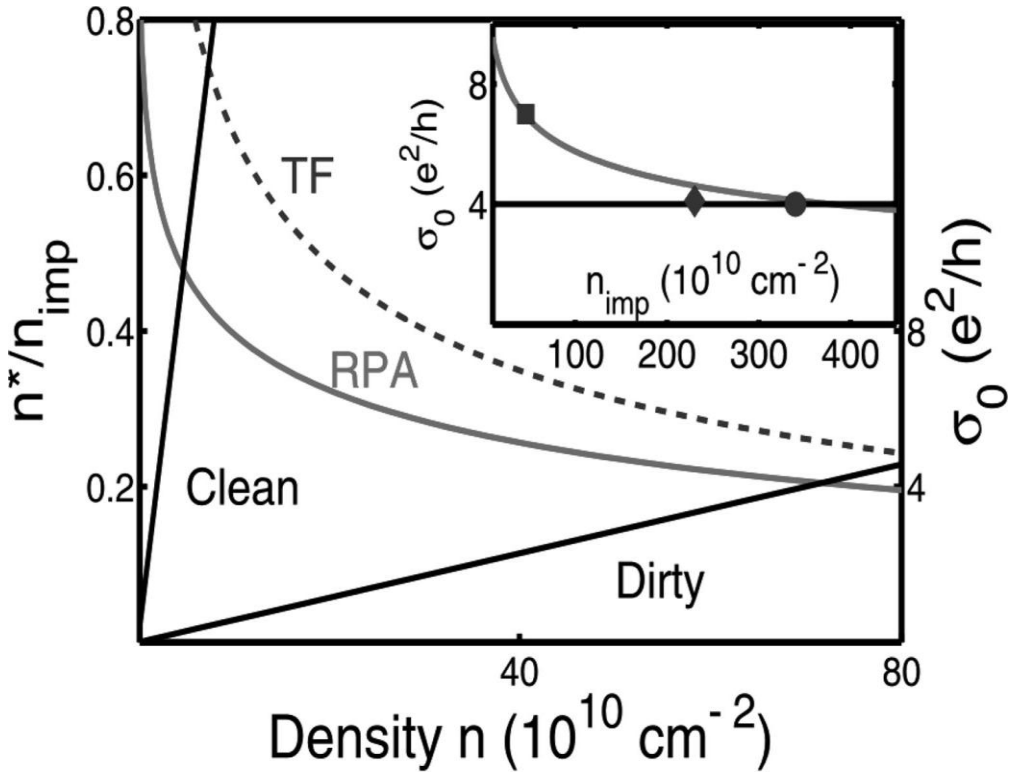
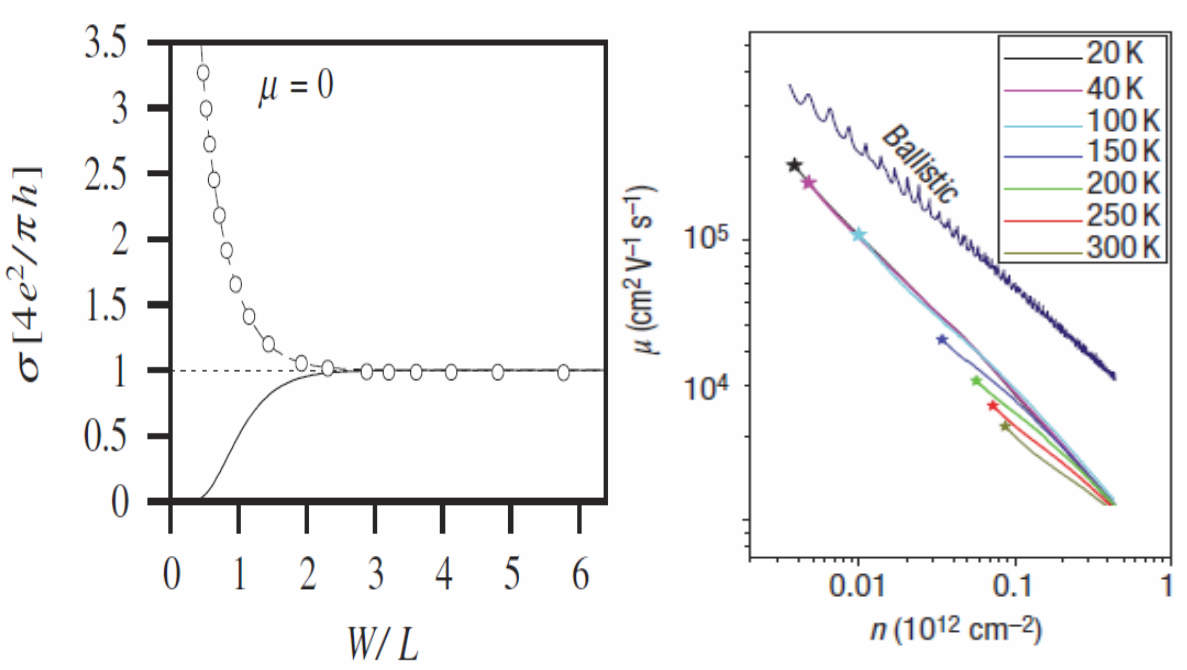


Figure 1.12 RPA and Thomas-Fermi (TF) as a function of carrier density: The points of intersection represent the self-consistent solution [From 58]

3) Ballistic transport

The charged impurities reduce the mean free path of charge carriers in graphene and make the transport diffusive. If this effect is ameliorated, graphene devices can possess very fast charge ballistic transport [59-60]. $4e^2/\pi h$ in the minimum conductivity at the Dirac point is the theoretically predicted value for ballistic transport.



(a) (b)

Figure 1.13 (a) Conductivity at the Dirac point as a function of the ratio of graphene strip and [From 59] (b) carrier density dependence on the mobility with different temperatures compared with Ballistic model [From 60]

CHAPTER 2 DEVICE ARCHITECTURES FOR IMPROVED AMORPHOUS POLYMER SEMICONDUCTOR THIN-FILM TRANSISTORS

2.1 Introduction

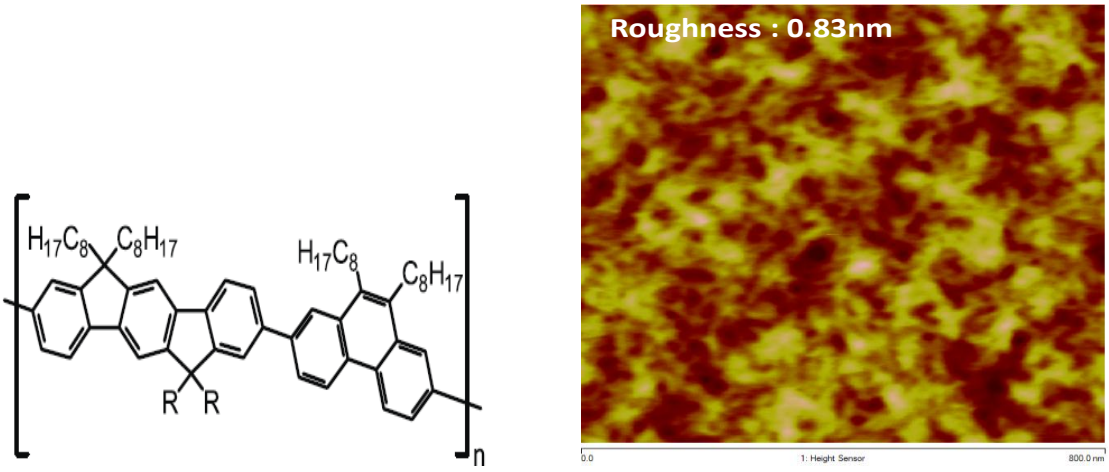
Amorphous polymeric semiconductors have characteristics that make them suitable for use in low-cost electronic circuits and photovoltaic devices [61]. These materials can be deposited using solution-based processes compatible with flexible substrates. Most reports of polymer transistors with mobilities > 0.1 cm^2/V-s involve liquid crystalline polymers [62-64]. Amorphous polymers with such large mobilities are relatively rare. In this chapter, we report on the performance characteristics of field-effect transistors with amorphous indenofluorene-phenanthrene copolymer semiconductor active layers with such mobilities [65].

The nature of the electrical contact between the source/drain electrodes and the semiconductor layer in OTFTs becomes an important influence on device performance as the channel length decreases [66-67]. Generally speaking, bottom gate and top contact (BGTC) geometry devices possess the least contact resistance because the effective area for charge injection in BGTC geometry is larger than in bottom gate and bottom contact (BGBC) geometry [68-69]. The BGTC structure device often possesses better performance compared to the BGBC structure when shadow-masking is used to deposit the contact metal. It has been reported that the use of self-assembled mono-layer (SAM) treatments and a recessed source/drain structure can improve the electrical contact

between the source/drain electrodes and the organic semiconductor layer [70-72]. However, there have been few reports on the combined effect of suitable surface treatments of source/drain electrodes and a recessed source/drain structure on the electrical contacts. The effects of surface treatments and recessed source/drain electrodes on the characteristics of indenofluorene-phenanthrene copolymer TFTs will be discussed below.

2.2 Amorphous indenofluorene-phenanthrene copolymer

A novel copolymer, indenofluorene-phenanthrene copolymer which was synthesized with poly(indenofluorene) homopolymer, consists of alternating components of substituted indenofluorene and phenanthrene, which is different from the structure of the side chain attached to the indenofluorene. Even though it has amorphous phase, the copolymer exhibits relatively high mobilities of > 0.01 cm^2/V-s. Such high mobilities result from insertion of transporting co-monomers into the polymer backbone, which can enhance carrier transport. In addition, the material has good solubility in common organic solvents such as toluene and chloroform. Figure 2.1 illustrates the molecular structures and atomic force microscopy (AFM) image of indenofluorene-phenanthrene copolymer.



(a) (b)

Figure 2.1 (a) Molecular structures and (b) AFM image of indenofluorene-phenanthrene copolymer

2.3 Indenofluorene-phenanthrene copolymer TFTs using recessed source/drain electrodes and dual-gate geometry

2.3.1 EXPERIMENTS

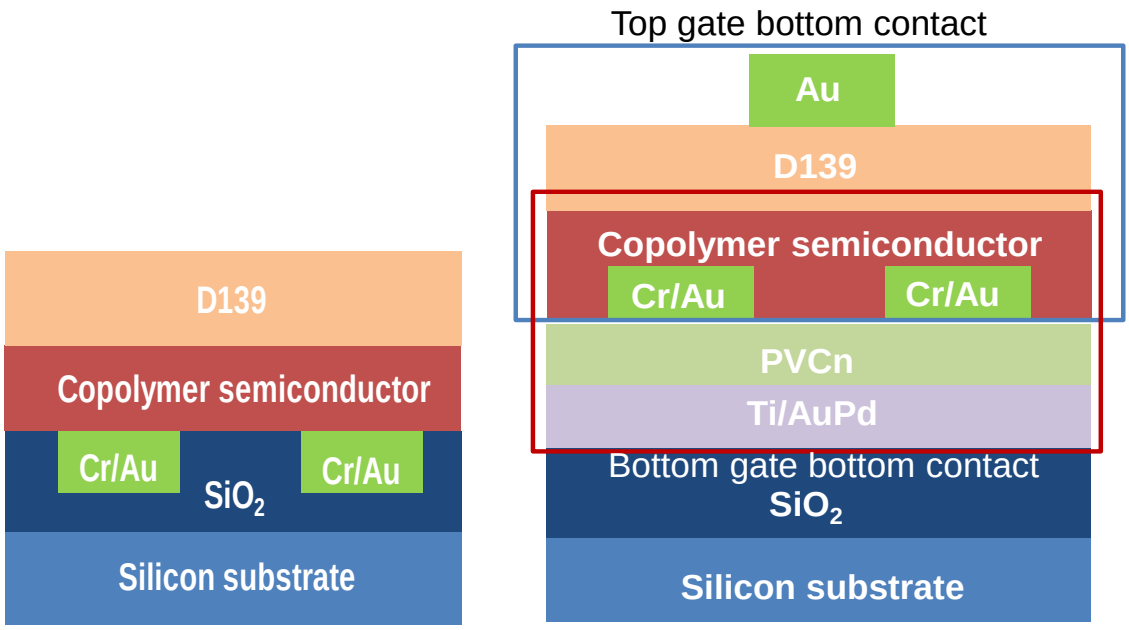
Figure 2.2 shows the schematic cross-section of organic TFTs based on indenofluorene-phenanthrene copolymer semiconductor using recessed source/drain electrodes and dual-gate geometry. Device fabrication started with an n-type silicon substrate with a resistivity of 1-10 Ωcm, also used as the bottom-gate electrode. This is thermally oxidized to result in a 160 nm thick silicon dioxide gate insulator. All samples were sonicated in acetone, methanol and isopropyl alcohol for 5 minutes each, dried with nitrogen gas, baked in a 120 ºC oven for 10 minutes to remove remaining water, and then exposed to UV ozone treatment for 5 minutes. Source/drain regions were patterned via a

photolithographic process for all samples. In half the samples, the silicon dioxide was first etched to a depth of 40 nm for 1 minute by a reactive ion etching to facilitate the formation of recessed source/drain contacts. A 2.5 nm chrome adhesion layer and a 37.5 nm gold layer were blanket deposited by thermal evaporation to define the source/drain electrodes by a standard lift-off process on all samples (both regular and recessed source/drain). Sets of devices from each group of samples were then treated with nitrobenzenethiol (NBT) to form a SAM [73-74]. These samples were immersed in a dilute NBT solution in chloroform (10 mM) for 1 hour, rinsed with ethanol to remove residual NBT, and then annealed at 120 ºC for 30 minutes. The samples were exposed to hexamethyldisilazane (HMDS) vapor at room temperature for 16 hours to improve the interface between the silicon dioxide gate dielectric and the organic polymeric semiconductor [75]. Both NBT and HMDS treatments were performed under an inert atmosphere.

The indenofluorene-phenanthrene copolymer solution was formed using toluene as the solvent (5 mg/mL concentration) with magnetic stirring at 50 ºC for 10 hours in an inert environment. The synthesis of the indenofluorene-phenanthrene copolymer has been described in detail by Schulte et al. [65]. The semiconductor film was formed by spin-coating for 45 seconds at 1600 rpm and then was pre-annealed at 110 ºC for 30 minutes. The thickness of semiconductor layer measured by elipsometer is ~70 nm. The as-supplied polymeric dielectric Merck® D139 was employed as a passivation layer. D139 was spin-coated onto the semiconductor layer for 5 seconds at 500rpm and then 50

seconds at 1000 rpm. After the spinning, the samples were cured by increasing the annealing temperature from 25 ºC to 130 ºC over 1 hour.

To fabricate the dual-gate devices, a 50 nm titanium and gold-palladium double layer as gate electrode was deposited onto a silicon dioxide barrier layer on a silicon substrate by e-beam evaporation. A poly(vinyl cinnamate) dielectric layer (0.5 wt% concentration in cyclopentanone) as bottom gate insulator was formed by spin-coating for 60 seconds at 1000 rpm. This layer was pre-annealed at 130 ºC for 25 minutes in nitrogen atmosphere and then cross-linked by exposing to UV radiation source of e-beam aligner (7.5 mW/cm^2 of intensity and 365 nm of wave length) for 10 minutes. After deposition of a 40 nm chrome and gold double layer as source/drain electrodes, the indenofluorene-phenanthrene copolymer semiconductor layer and D139 layer as top gate insulator were spin-coated in order. Finally, a 50nm gold layer as top gate electrode was deposited by thermal evaporation. The device fabrication was completed with a thermal post-anneal at 140 ºC for 10 hours. The spin-coating and thermal annealing of semiconductor and D139 layers were performed under nitrogen atmosphere.



(a) (b)

Figure 2.2 The schematic cross-section of organic TFTs based on indenofluorene-phenanthrene copolymer semiconductor using recessed source/drain electrodes and dual-gate geometry. Copyright 2012, Elsevier

2.3.2 RESULTS

Figure 2.3 (a) and (b) show the output characteristics of an amorphous indenofluorene-phenanthrene copolymer TFT using elevated source/drain electrodes and recessed source/drain electrodes without surface treatment. With the recessed source/drain electrodes, the on-current level increased by about a factor of 4 and the field-effect mobility increased from 0.018 cm^2/V-s to 0.055 cm^2/V-s as compared to the elevated structure. The super-linear behavior seen as low drain voltages in the elevated contact structure is attributed to a high injection barrier, which is reduced substantially by the adoption of recessed contacts, as shown in Figure 2.3.

In order to further investigate the combination effect of recessed source/drain electrodes and the surface treatment of the electrodes, non-treated and NBT-treated samples based on both recessed and elevated source/drain structure have been compared. SAM surface treatments are expected to reduce contact resistance by improving the physical contact between the metal and semiconductor [70-71]. After applying surface treatments, the device performance for surface-treated samples is improved in both the recessed and elevated source/drain geometries as shown in Figure 2.3 (c) and Figure 2.3 (d). The device employing surface-treated, recessed source/drain possesses a field-effect mobility of 0.144 cm^2/V-s, sub-threshold swing (S.S.) of 1.25 V/decade and on-off current ratio in excess of 10^5 in air.

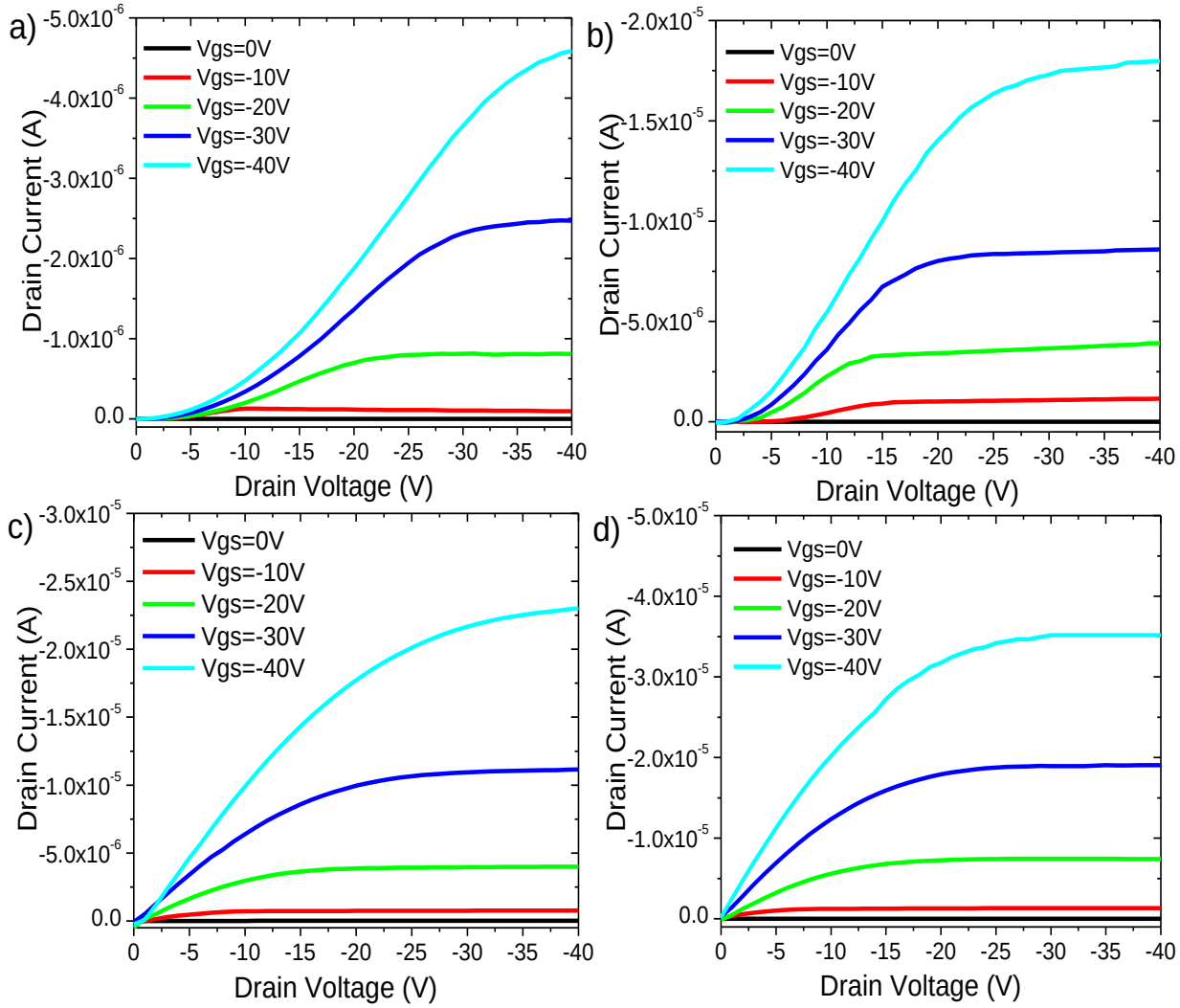
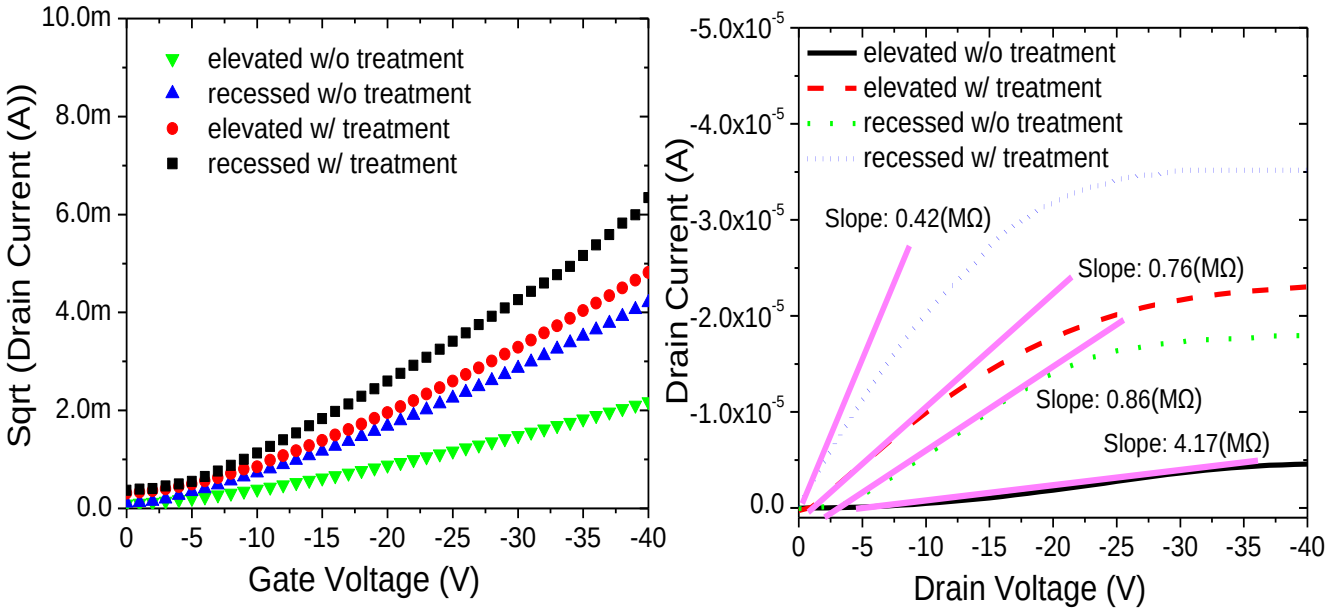


Figure 2.3 the output characteristics of an amorphous indenofluorene-phenanthrene copolymer TFT using (a) elevated source/drain electrodes without treatment (b) recessed source/drain electrodes without treatment (c) elevated source/drain electrodes with treatment and (d) recessed source/drain electrodes without treatment. Copyright 2012, Elsevier

Figure 2.4 (a) shows the square root of drain current versus gate voltage with different conditions. Effective mobilities extracted by Figure 2.4 (a) increase due to the improved electrical contact. The use of NBT surface treatment, as shown in Figure 2.4 (b), improves hole injection between gold source/drain electrodes and the organic semiconductor layer [76-77]. Significantly, the combination of the use of surface treatments and the recessed source/drain geometry improves the effective mobility of amorphous indenofluorene-phenanthrene copolymer TFTs, to about a factor of 9 higher than the non-treated, elevated source/drain sample as shown in Figure 2.4 (b)



(a) (b)

Figure 2.4 (a) The square root of drain current vs. gate voltage with different conditions and (b) the effect of the surface-treated, recessed source/drain geometry on contact resistance of amorphous indenofluorene-phenanthrene copolymer TFT. Copyright 2012, Elsevier

The total resistance in TFT devices is the sum of the contact resistance and channel resistance [76-77]. If channel length decreases, the intrinsic channel resistance decreases and the relative influence in the contact resistance increases. Therefore, device characteristics such as the apparent field-effect mobility are influenced by significant contact resistance [77-79]. In order to investigate the dependence of contact resistance on channel length, a transmission line method can be used to extract the value of contact resistance [76-78]. The contact resistance can be calculated by determining the device on-resistance from the linear region mode operation and plotting the width-normalized on-resistance as a function of channel length for different gate voltages. The width-normalized contact resistance is extracted at the y-axis intercept of the extrapolated linear fits of the different gate voltages. Figure 2.5 (a) shows the width-normalized device resistance as a function of channel length at the gate voltages of -20V, -30V and -40V with the drain-source voltage of -2V. This was extracted from output characteristics curves on devices with channel lengths ranging from 4 μm to 50 μm. The width-normalized contact resistance was extrapolated from the graph to be 1275 Ωcm for devices employing recessed contacts modified with NBT surface treatment. Figure 2.5 (b) shows the width-normalized resistances as a function of gate and drain voltages in recessed source/drain with surface treatment and elevated source/drain without surface treatment. Width-normalized resistances of a non-treated TFT with elevated contacts are strongly influenced by drain voltage in linear mode operation. The schottky barrier is attributed to a high injection barrier, which influences the effective mobility. Furthermore, width-normalized resistances decrease with increasing drain voltage

compared to surface-treated, recessed source/drain TFT, indicating there is the point of certain threshold of injection barrier.

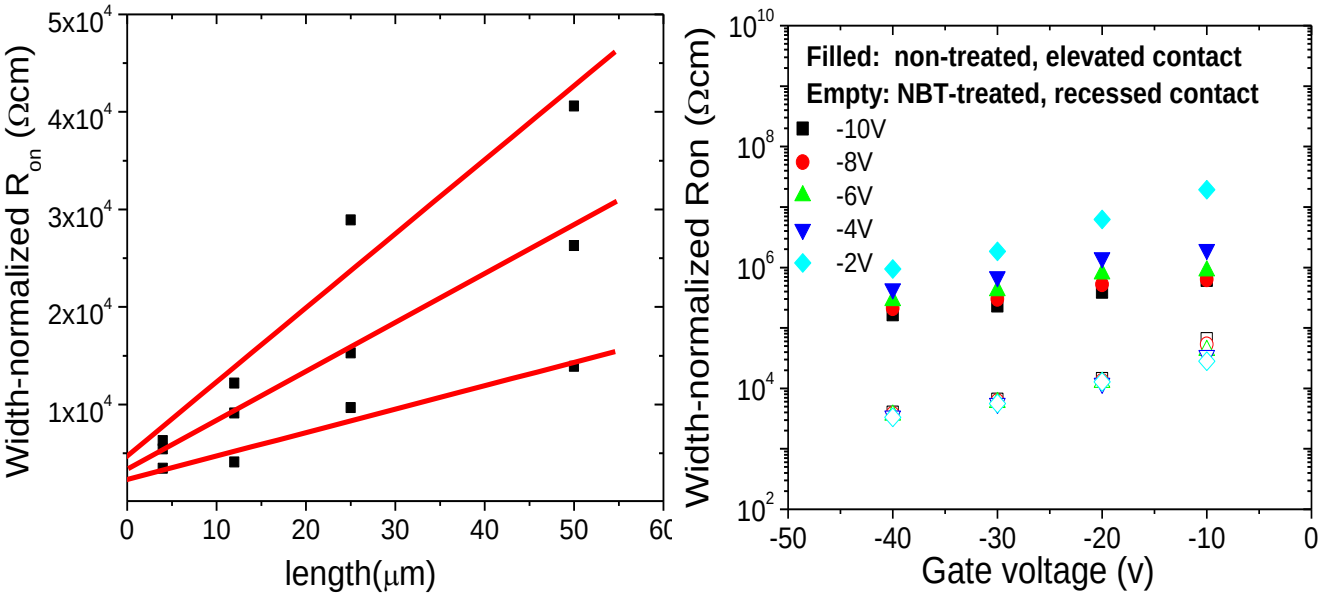


Figure 2.5 (a) Width normalized resistance as a function of channel length at the gate voltages with fixed drain voltage using recessed source/drain electrodes with treatment and (b) width-normalized resistances as a function of gate and drain voltage in recessed source/drain with treatment (filled) and elevated source/drain without treatment (empty). Copyright 2012, Elsevier

Dual-gate TFTs have exhibited improved performance in all these cases with the off-current being usually lower, due to better gate control, and the on-current and the sub-threshold behavior improved compared to single-gate devices. The dual-gate geometry can result in two accumulation channels. Furthermore, carrier concentration or the channel conductivity of a semiconductor in a dual-gate mode operation can be effectively controlled through the voltages applied independently to the top and bottom TFT gate electrodes over single-gate mode operation [80-82].

Figure 2.6 shows the output and transfer characteristics in the top-gate, bottom-gate and dual-gate modes of a dual-gate indenofluorene-phenanthrene copolymer TFT at the gate voltages ranging from -40V to 40V with the drain-source voltage of -40V. These TFTs possess a field-effect mobility of 0.2cm2/V-s when measured in the top-gate mode and 0.09cm^2/V-s in the bottom-gate mode in air. The current of the top-gate device is lower than that of the bottom-gate device because polymer gate dielectric as top-gate insulator is thicker and has a lower capacitance per unit area (4 nF/cm^2) compared to silicon dioxide as bottom-gate insulator (20 nF/cm^2). The characteristics of the interface have a significant influence on the measured mobility [83-84]. The fabrication sequence of the top-gate device allows the use of an in-situ process in which the semiconductor layer and the top-gate insulator layer can be deposited sequentially under an inert environment. For this reason, better quality interfaces can be obtained from top-gate devices. In addition, the effective area for charge injection in the top-gate bottom-contact device is larger than that in BGBC device, leading to improved contact properties. Dual-gate mode operation results in improved performance such as increased on-current, reduced threshold voltage (Vth), improved S.S. and increased on-off current ratio compared to either single gate mode as shown in Figure 2.6. This is because interaction between charge carriers and interface between a semiconductor and a gate insulator layer is reduced.

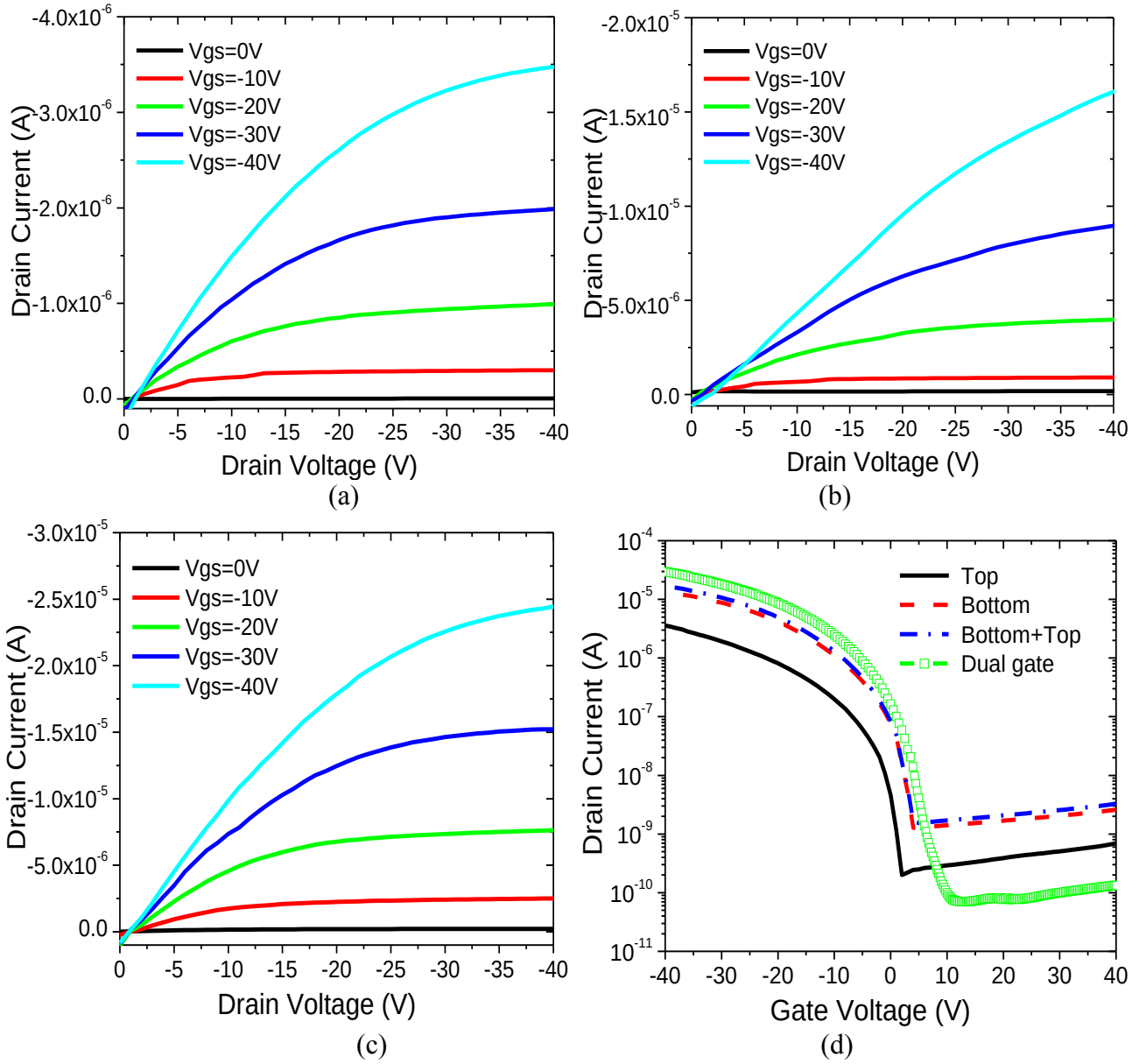
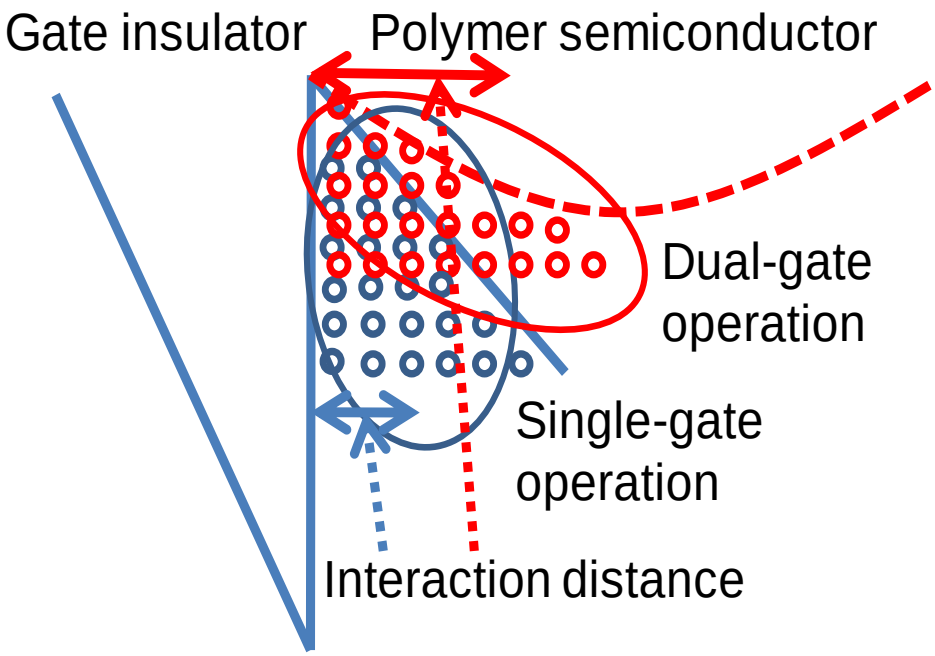


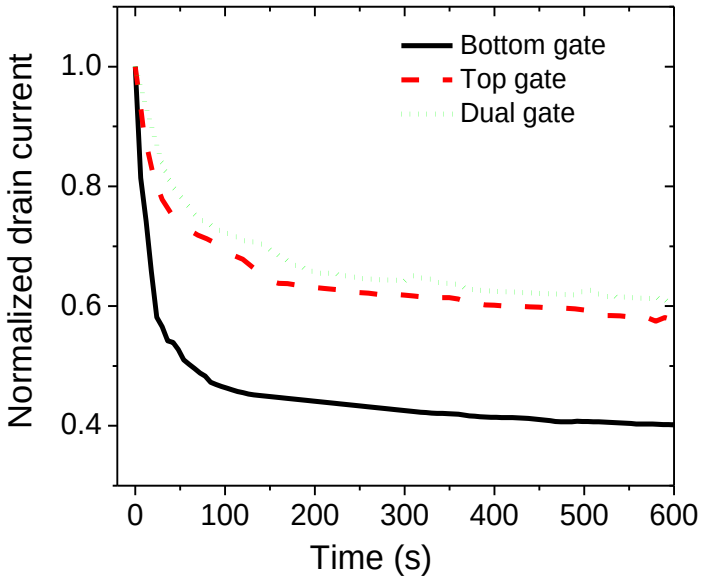
Figure 2.6 The output characteristics in the (a) top-gate, (b) bottom-gate and (c) dual-gate modes and (d) the transfer characteristics of a dual-gate indenofluorene-phenanthrene copolymer TFT at the gate voltages ranging from -40V to 40V with the drain-source voltage of -40V. Copyright 2012, Elsevier

Figure 2.7 (a) shows the schematic illustration of interfacial energy band diagram in case of single-gate mode vs. dual-gate mode. In single-gate devices, charge carriers are more highly confined, leading to enhanced interaction with interface. When the other gate bias is applied, interaction distance between charge carriers and interface in dual-gate mode becomes increased over singe-gate mode due to the band bending. It means that interface characteristics in dual-gate mode are improved due to the reduced interaction of charge carriers. Horowitz et al. reported that the mobility of charge carriers in organic FETs is lower closer to the interface compared to the bulk [85]. This is because of a greater interaction with the interface. The same effect is one of the factors responsible for the improved performance of dual-gate mode operation. Improved interface characteristics lead to improved S.S. and reduced Vth including increased on-current and on-off current ratio. Improved S.S. and reduced Vth can also explain why the current density from a dual-gate device is larger than the sum of current densities of both top- and the bottom-gate devices, as shown in Figure 2.6 (d).

We note that other reasons have been provided for improved performance of dual-gate devices such as gate screening effects and shift of Vth [80, 86]. Such effects also result in improved performance of dual-gate devices. When a constant voltage stress is applied in each mode of operation, dual-gate mode exhibits greater stability than the single-gate modes as shown in Figure 2.7 (b).



(a)



(b)

Figure 2.7 (a) The schematic illustration of interfacial energy band diagram in case of single-gate mode vs. dual-gate mode and (b) the electric-bias stability characteristics of top, bottom and dual-gate mode in amorphous indenofluorene-phenanthrene copolymer FETs. Copyright 2012, Elsevier

This is also a consequence of improved interface characteristics due to the reduced interaction of charge carriers with the interfaces. These results demonstrate that high mobilities can be achieved in amorphous polymer field-effect transistors. The mobility values we report are comparable to those reported for regioregular poly(3-hexyl thiophene), a liquid crystalline semiconductor that has been extensively investigated for over a decade by many groups [62-64, 87]. Our work further demonstrates the importance of contact engineering on device performance for this class of materials. The mobilities achieved at channel lengths of 4 μm suggest that such semiconductors will be useful in a number of applications such as displays.

2.4 Indenofluorene-phenanthrene copolymer TFTs employing hybrid high-k / low-k dielectrics

One of the keys realizing high-performance organic semiconductor devices is the choice of gate dielectric. Hulea et al. focused on the mobility characteristics of single crystal rubrene FETs with different dielectric constants of gate insulator and reported that the mobility decreases with increasing dielectric constant [88]. This was attributed to Fröhlich polaron effects [88]. The operating voltage of OFETs often exceeds 40V when low-k gate dielectrics are employed. For this reason, high dielectric constant (high-k) materials have been used as gate insulator to enhance the accumulation of charge carriers at a low gate voltage. However, for reasons described above, using a high-k dielectric as gate insulator in OFETs based on low gate voltage operation results in decreased

mobility. Hence, hybrid dielectric layers using both a high-k and a low-k dielectric might help bring down operating voltage while maintaining high mobility.

2.4.1 EXPERIMENTS

In order to make low gate-voltage operation devices, zirconium dioxide (ZrO_2) dielectric was chosen as a gate insulator. A ZrO_2 solution was synthesized with a sol-gel chemistry method by dissolving zirconium chloride and zirconium isopropoxide isopropanol powers (1.158:1.927) in 2-methoxyethanol (0.5M concentration) with magnetic stirring at room temperature for 6 hours in an inert environment. By a suitable selection of precursors and optimized process conditions, improved ZrO_2 dielectric layers having better surface morphology and low leakage current can be obtained. In particular, slow evaporation of solvent under the inert atmosphere and uniform thermal-annealing process strongly influenced device characteristics. The high-k dielectric layer was formed by spin-coating for 60 seconds at 4000 rpm and followed to keep in the nitrogen environment for 1 hour to evaporate the residual solvent with gradual rate, and then was pre-annealed at 500 ºC for 1 hour in air atmosphere. This process was repeated to deposit double layer of ZrO_2. The second layer of ZrO_2 addressed uniformity issues with the first layer. Bi-layer dielectrics exhibit lower defect-related leakage current as pinholes or other defects formed during the first deposition may be moderated by the second layer.

Even though ZrO_2 gate insulator layers are well-optimized, using high-k dielectric in OFETs based on low gate voltage operation causes a higher leakage current and

decreased mobility while the breakdown voltage is increased. For this reason, the combination of high-k and low-k was employed in an attempt to suppress leakage current. One such low-k material that was employed is poly(vinyl cinnamate). By controlling the concentration of poly(vinyl cinnamate) and the spin-speed of deposition, the twin goals of maintaining a high average dielectric constant as well as lower leakage current densities were achieved. A poly(vinyl cinnamate) solution was formed using cyclopentanone as the solvent (0.5 wt% concentration) with magnetic stirring at room temperature for 12 hours in an inert environment. Ultra-thin organic dielectric interface layer was formed by spin-coating for 30 seconds at 4000 rpm and then was pre-annealed at 100 ºC for 1 hour in nitrogen. In order to apply photolithography process on poly(vinyl cinnamate) layer for short channel devices, it was cross-linked by exposing to UV radiation source of e-beam aligner (7.5mW/cm^2 of intensity and 365 nm of wave length) for 10 minutes. This cross-linking reaction makes poly(vinyl cinnamate) become insoluble in solvents.

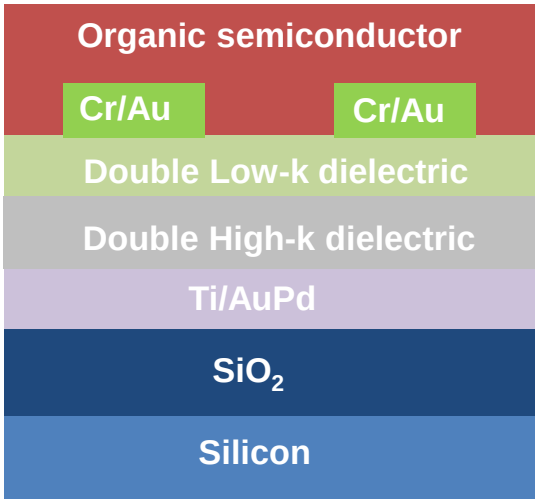


Figure 2.8 The schematic cross-section of indenofluorene-phenanthrene copolymer TFT employing hybrid high-k/low-k dielectrics

2.4.2 RESULTS

Figure 2.9 (a) and (b) show the output and transfer characteristics in indenofluorene-phenanthrene copolymer TFT employing hybrid high-k/low-k dielectrics at the gate voltages of 5V with the drain-source voltage of 5V. These TFTs exhibit that good output characteristic with low electrical contact resistance and on-off current ratio of $> 10^4$ at the saturation regime with small hysteresis. The extracted field-effect mobility increases with gate voltage to about 0.11 cm^2/V-s and leakage current is less than 1nA, as shown in Figure 2. 9 (c) and (d).

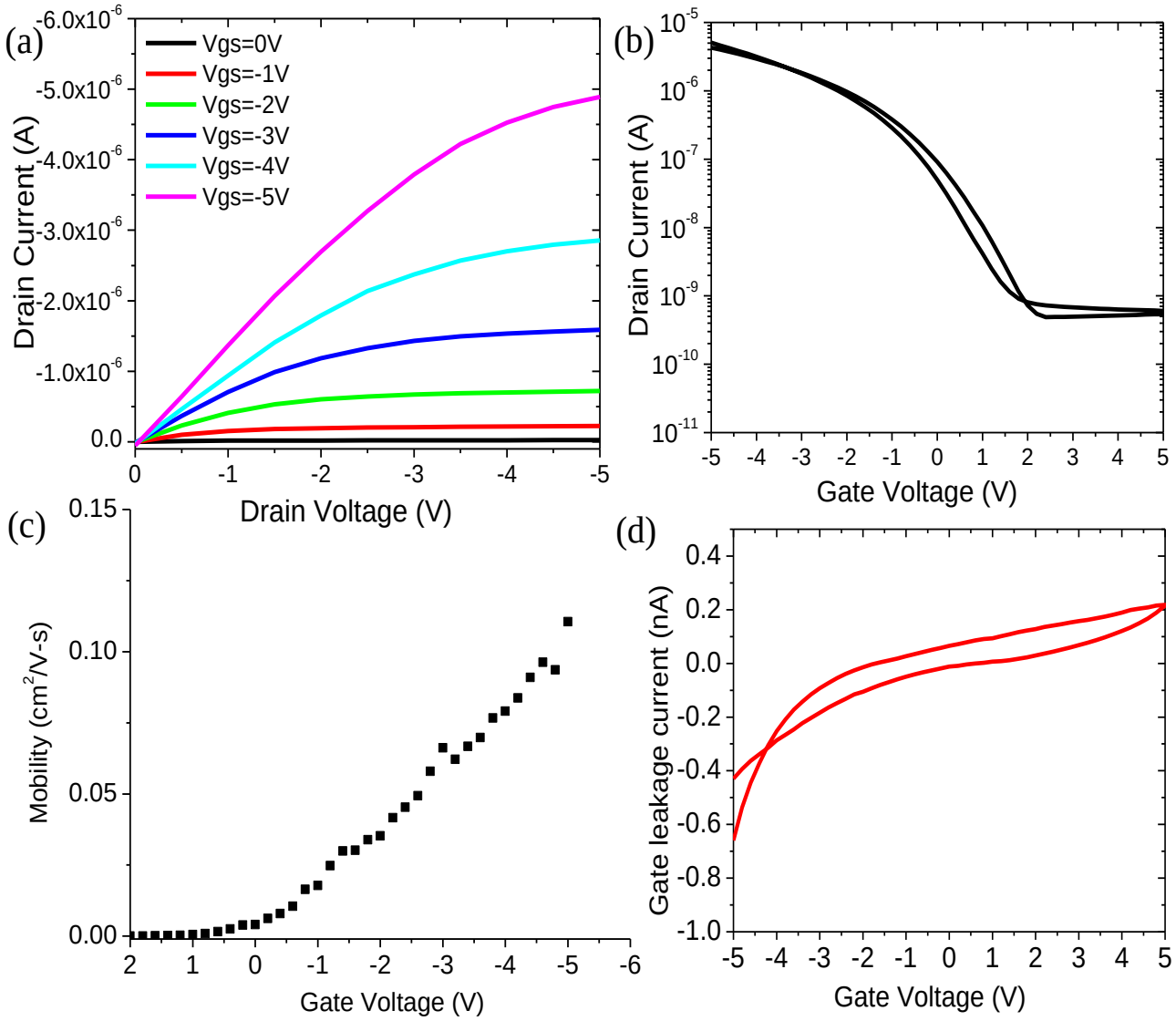


Figure 2.9 (a) The output (b) transfer characteristics (c) extracted field-effect mobility and (d) gate leakage current in indenofluorene-phenanthrene copolymer TFT employing hybrid high-k/low-k dielectrics at the gate voltages of 5V with the drain-source voltage of 5V.

2.5 Conclusions

In summary, the bottom gate bottom contact amorphous polymer semiconductor TFTs based on indenofluorene-phenanthrene copolymer exhibit a field-effect mobility of up to 0.144 cm^2/V-s and a width-normalized contact resistance of 1275 Ωcm in air. In addition, we fabricated dual-gate indenofluorene-phenanthrene copolymer TFTs, which possess enhanced gate control as well as less instability caused by electrical bias stress compared to single gate TFT mode operation. Device characteristics in dual-gate mode were improved due to the reduced interaction of charge carriers with interface states. The use of hybrid high-k/low-k dielectrics results in low-voltage operation with less leakage current in these TFTs. The combination of suitable surface treatments of source/drain contact electrodes and the recessed source/drain geometry and device architecture of dual-gate configuration and hybrid high-k/low-k dielectrics are the key to realizing such better device performance characteristics required for flexible electronics.

CHAPTER 3 DEVICE PHYSICS OF POLYMER THIN-FILM TRANSISTORS BASED ON DIKETOPYRROLOPYRROLE-NAPHTHALENE COPOLYMER AND CHARGE TRANSPORT

3.1 Introduction

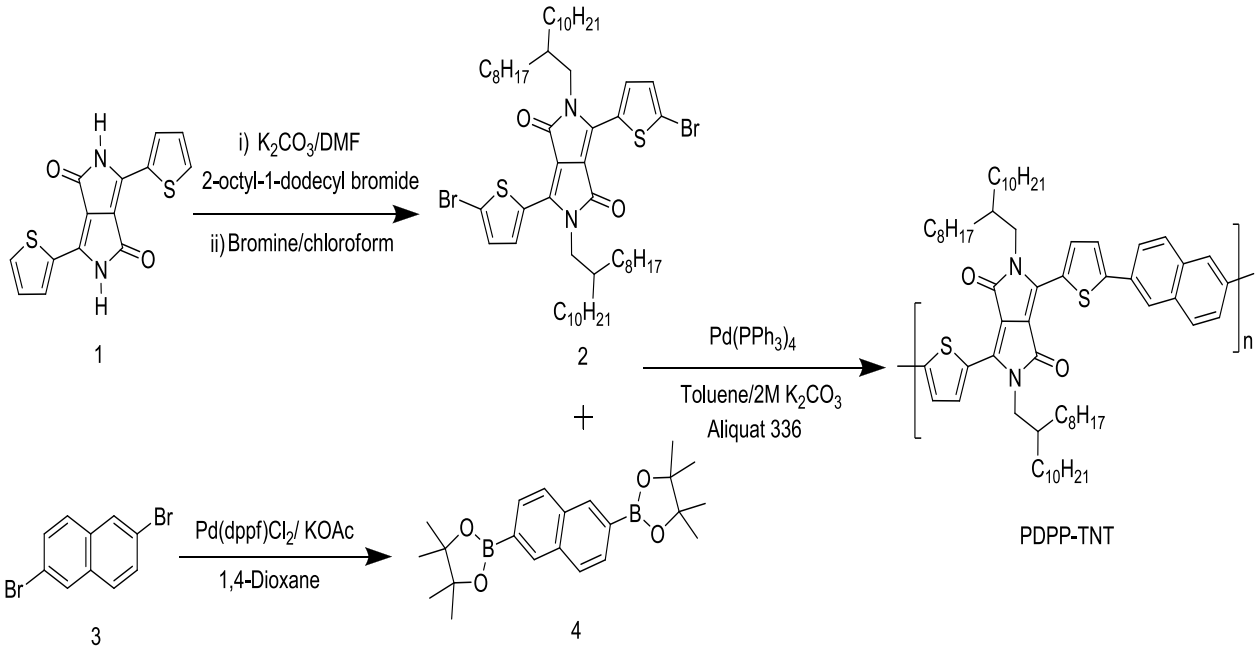
Since the first report that the use of regioregular conjugated polymer semiconductors can result in significantly improved field-effect mobilities in FETs [64], there have been numerous reports on ordered polymeric semiconductors which possess relatively high mobilities of more than 0.1 cm^2/V-s [9, 62-63, 89]. Molecular weight, ordering, annealing temperatures and overpressure conditions and device architectures influence device performance [90-92]. Recently, we fabricated high mobility polymer thin-film transistors (TFTs) using the diketopyrrolopyrrole-naphthalene copolymer (PDPP-TNT) semiconductor [93]. These devices possess a field-effect mobility of up to 1 cm^2/V-s with low contact resistance and are easily processible and relatively stable. Key to realizing such high mobilities in this material are molecular design, the use of suitable surface treatments of the source/drain contact electrodes and device architectures, particularly top-gate configurations.

There have been many studies on charge transport in OFETs and nearly all of them have utilized steady-state or direct-current device measurements as a function of parameters such as temperature, carrier concentration, and electrical-field [94-96]. we measure the velocity distributions in OFETs and show that this can provide additional information compared to steady-state measurements alone [97-99]. Specialized time-domain measurements, performed while keeping the RC-time constant of the

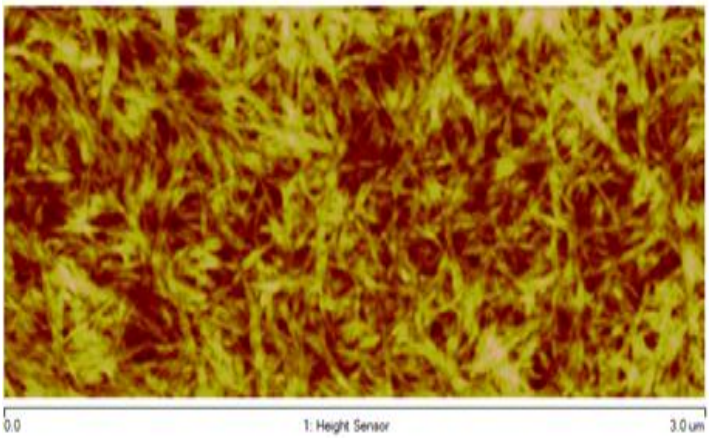
measurement circuit small, permit the extraction of non-quasi-static velocity distributions of charge carriers [99]. A step-voltage pulse applied to the source electrode injects charge carriers into the channel. The time-dependent drain current is measured through a variable resistor, and yields a distribution of arrival times of charge carriers at the drain electrode. In this chapter, we investigate the device performance and charge transport of dual-gate TFTs using PDPP-TNT semiconductor in steady-state and under non-quasi-static conditions.

3.2 Diketopyrrolopyrrole-naphthalene copolymer

This subsection discusses basic details of the synthesis of PDPP-TNT as described by Dr. Prashant Sonar who is our close collaboration. Figure 3.1 shows the synthesis process and AFM image of PDPP-TNT. Compound 2, 5-dihydro-1, 4-dioxo-3, 6-dithienylpyrrolo [3, 4-c]-pyrrole (1) was readily synthesized using reported procedure [93], which was then converted to 3,6-bis-(5-bromo-thiophen-2-yl)-N,N'-bis((octyldodecyl)-1,4-dioxo-pyrrolo[3,4-c]pyrrole (2) via alkylation and bromination respectively. 6-Bis(4,4,5,5-tetramethyl-1,3,2-dioxabrolan-2-yl)naphthalene (4) was obtained from 2,6-dibromonaphthalene (3) using bis(pinacolato)diboron, PdCl2(dppf) and KOAc in 1,4-dioxane. Suzuki polymerization of compounds 3 and 4 results polymer PDPP-TNT in 74% yield.



(a)



(b)

Figure 3.1 (a) Synthesis [From 93] and (b) AFM image of PDPP-TNT

PDPP-TNT was purified by sequential Sohxlet extraction using methanol, and acetone hexane in order to remove catalytic impurities and oligomer fractions from the bulk polymer sample. Finally, the polymer was obtained by dissolving in chloroform, followed by precipitation from methanol. The number average (Mn) and weight average

molecular weight (Mw) calculated by gel permeation chromatography (GPC) is 63,750 and 91,310 g/mol respectively using polystyrene standards. The optical band gap (Egopt) calculated from the solid state absorption onset is ~ 1.50 eV. The calculated HOMO value of PDPP-TNT is ~ 5.29 eV from the oxidation onset (0.89V). LUMO value calculated from the difference between the Egopt (1.50 eV) and HOMO value (5.29 eV) is 3.79 eV. A DPP-based polymer, PDBT-co-TT, which has an electron accepting diketopyrrolopyrrole (DPP) unit and an electron donating thieno[3,2-*b*]thiophene (TT) unit showed high hole mobility of up to 1 cm^2/V.s. Naphthalene is one of the most common fused ring aromatic structures with linear π-systems used as a building block for polymer semiconductors. Fused ring structures comprising inner naphthalene moiety, such as naphthalene-bis(dicarboximide) and naphthaodithiophene (NDT) have been used for constructing n-type and p-type polymers. PDPP-TNT is soluble in most of the common organic solvents due to a long branched alkyl, 2-octyl-1-dodecyl substituted on the N-atom of the DPP.

3.3 High mobility top-gate and dual-gate polymer TFTs based on diketopyrrolopyrrole-naphthalene copolymer

3.3.1 EXPERIMENTS

Figure 3.2 shows the schematic cross-section of a dual-gate polymer TFT possessing a PDPP-TNT semiconductor active layer. Device fabrication started with an

n-type silicon substrate with a resistivity of 1-10 Ω cm, also used as the bottom-gate electrode. This is thermally oxidized to result in a 200 nm thick silicon dioxide bottom-gate insulator. All samples were sonicated in acetone, methanol and isopropyl alcohol for 5 minutes each, dried with nitrogen gas, baked in a 120 ºC oven for 10 minutes to remove remaining water, and then exposed to UV ozone treatment for 3 minutes. A 52.5 nm thick chrome/gold (2.5 nm/50 nm) bi-layer as a source and drain electrode was deposited by thermal evaporation. Samples were treated with NBT to form SAM. These samples were immersed in a dilute NBT solution with chloroform (0.2 mM) for 3 hours, then rinsed with ethanol to remove residual NBT, and then annealed at 130 ºC for 30 minutes. The samples were exposed to the octyltrichlorosilane (OTS-8) vapor at 110 ºC for 3 hours and then treated with isopropyl alcohol to improve the interface between the silicon dioxide gate dielectric and the polymer semiconductor. Both NBT and OTS-8 treatment were performed under an inert atmosphere.

The PDPP-TNT solution was formed using chloroform as the solvent (7 mg/mL concentration) with magnetic stirring at 53 ºC for 6 hours in an inert environment. The semiconductor film was formed by spin-coating for 50 seconds at 1500 rpm and then pre-annealed at 120 ºC for 30 minutes. Next, the as-supplied Polymeric Merck® dielectric (D139) as a top-gate insulator was spin-coated onto the PDPP-TNT layer for 5 seconds at 500 rpm and then for 50 seconds at 1500 rpm. After spinning, it was cured gradually from 25 ºC to 130 ºC over 1 hour. This process was repeated to deposit as second layer of the top-gate insulator. Finally, a 45 nm thick gold as a top-gate electrode was deposited by thermal evaporation. The device fabrication was completed with thermal annealing at

140 ºC for 10 hours. The spin-coating and thermal annealing of the PDPP-TNT and D139 were performed under nitrogen atmosphere. All samples were characterized by parameter analyzer and measured in air. Bottom- and top-gate TFT characteristics were measured separately and dual-gate operation measurements were made by applying a gate bias on both bottom- and top-gates simultaneously.

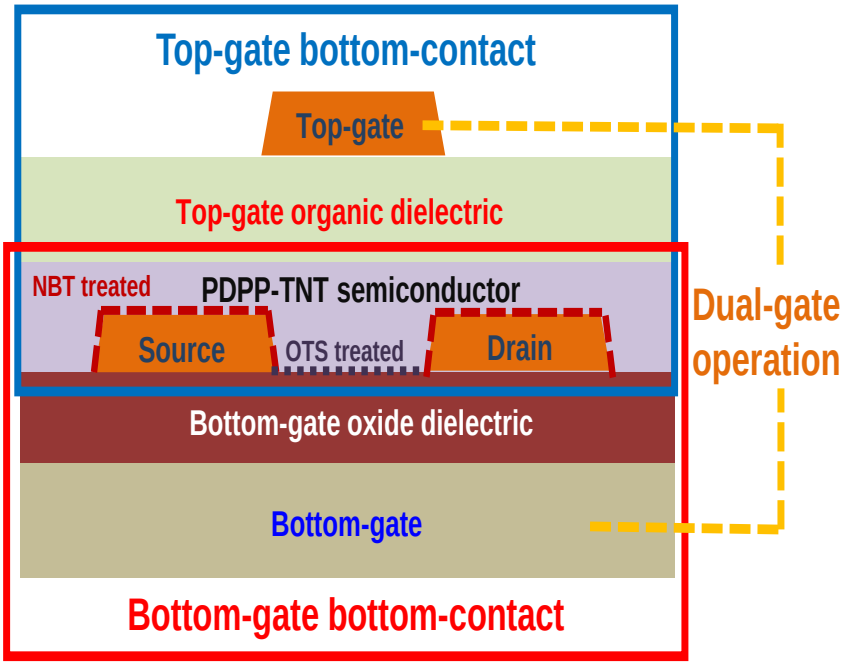


Figure 3.2 The schematic cross-section of a dual-gate polymer TFT possessing a PDPP-TNT semiconductor active layer

3.3.2 RESULTS

Figure 3.3 shows the output and transfer characteristics of PDPP-TNT TFT employing top-gate configuration. Due to the combined effects of OTS-8 and NBT treatments as well as thermal annealing, improved device performance was obtained. The

extracted width-normalized contact resistance is ~8.4 kΩcm. The contact resistance can be calculated by determining the device on-resistance from the linear region mode operation and plotting the width-normalized on-resistance as a function of channel length for different gate voltages [100]. The contact resistance is not expected to be dominant because the channel length is very long and a SAM treatment improved the electrical contact between the electrodes and the semiconductor [73].

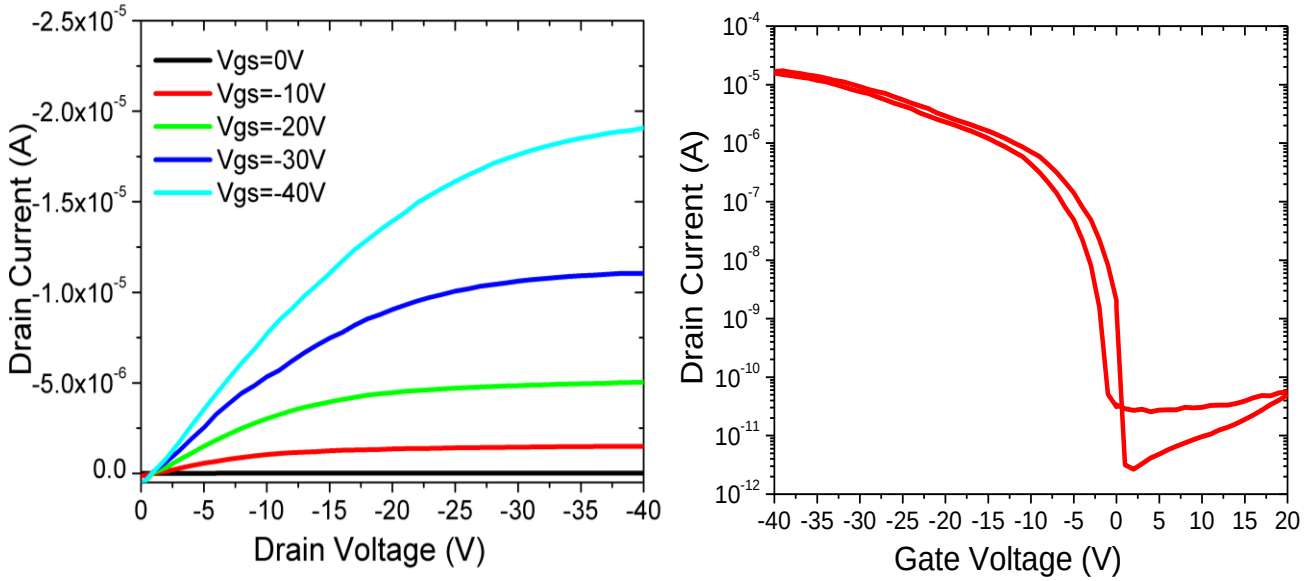


Figure 3.3 (a) the output and (b) transfer characteristics of PDPP-TNT TFT employing top-gate configuration. Copyright 2011, American Institute of Physics

Figure 3.4 shows the saturation field-effect mobility and the square root (SQRT) of drain current versus gate voltage of a PDPP-TNT TFT employing top-gate configuration. The device exhibits a field-effect mobility of up to 0.98 cm^2/V-s with low Vth, which is comparable to reported vapor-deposited small molecule based organic semiconductors

[101-103]. The trap density of states calculated by S.S. value in PDPP-TNT TFTs is 3.17×10^{11} $cm^{-2}eV^{-1}$ [104]. SAM surface treatments result in increasing the molecular ordering by modifying the surface energy at the interface, which leads to better molecular packing which in turn leads to better charge carrier injection and higher effective mobilities [73, 75]. The field-effect mobility has increased from 0.42 $cm^2/V\text{-}s$ with no annealing and no surface treatment to 0.98 $cm^2/V\text{-}s$ after surface treatment and annealing at 140 ºC as shown in Figure 3.5. Annealing also results in a reduced hysteresis window (from 8.7 V to 1.2 V) as well as a much lower off-current. The aging characteristics in air for 7 days are relatively small changes and are reversible by repeating the annealing step as shown in Figure 3.6.

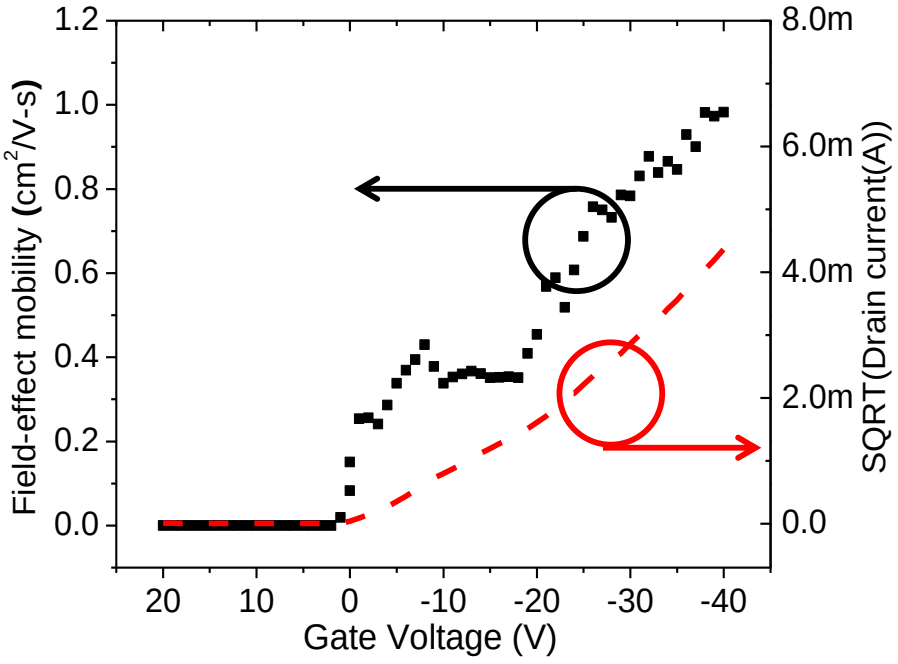


Figure 3.4 The saturation field-effect mobility and the square root of drain current versus gate voltage of a PDPP-TNT TFT employing top-gate configuration. Copyright 2011, American Institute of Physics

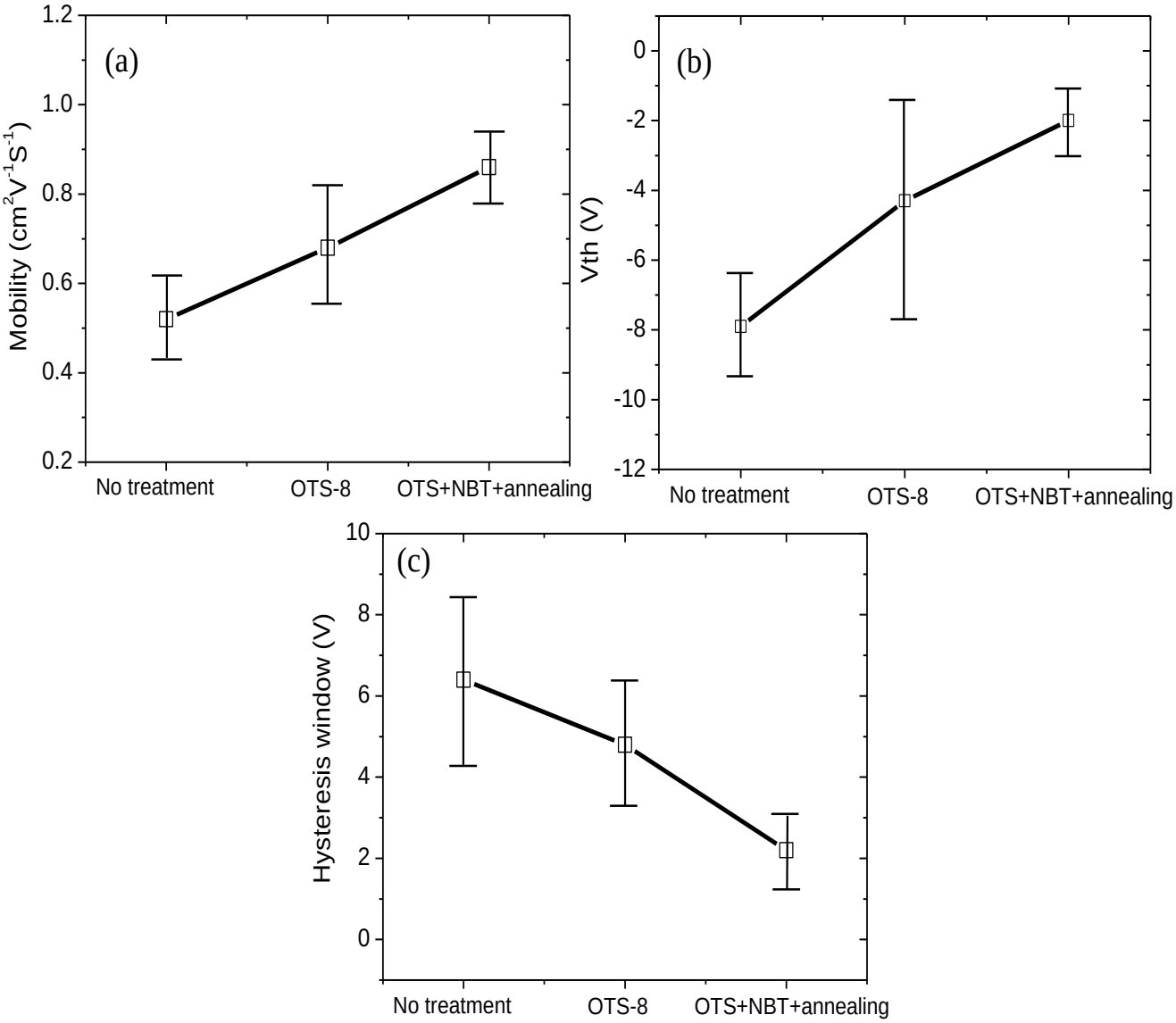


Figure 3.5 (a) The mobility (b) Vth and (c) hysteresis characteristics of PDPP-TNT TFT with different treatment conditions

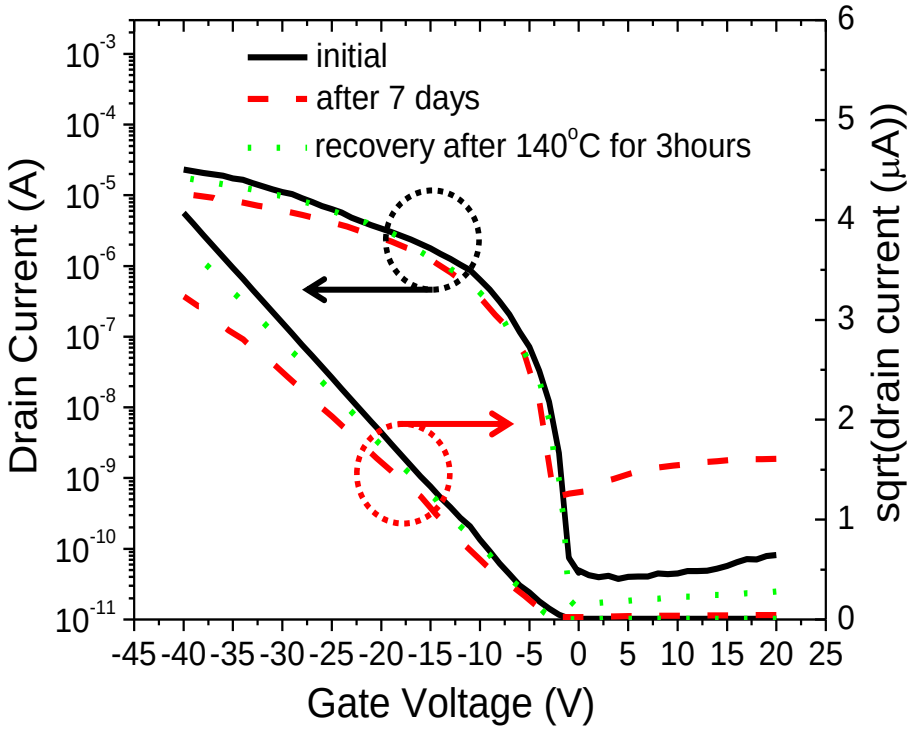
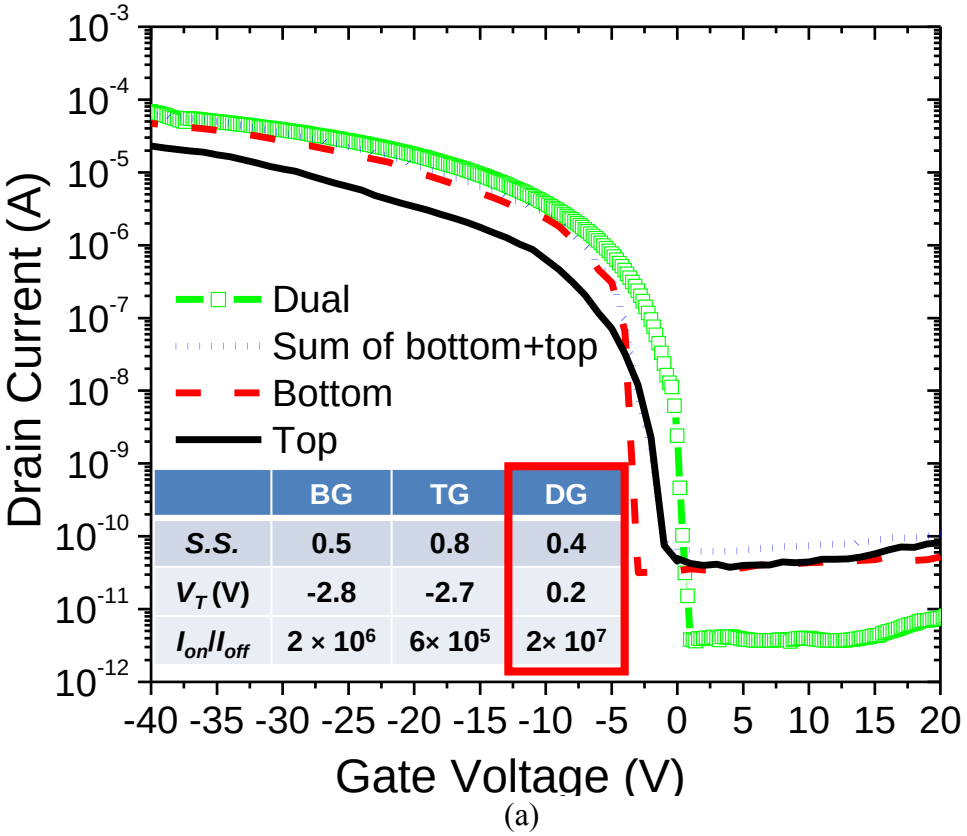


Figure 3.6 The aging characteristics in air for 7 days of PDPP-TNT TFT

Figure 3.7 (a) shows the transfer characteristics in the top-gate, bottom-gate and dual-gate modes of a dual-gate PDPP-TNT TFT. Dual-gate mode operation results in the lowest Vth and improvements in S.S. and on-off current ratio compared to a top-gate or a bottom-gate. The Vth in dual-gate mode was decreased to 0.2 V compared to that of the single-gate mode, -2.8 V (bottom) and -2.7 V (top) and S.S. was improved to 0.39 V/decade compared to 0.5 V/decade (bottom) and 0.81 V/decade (top). In addition, the on-off current ratio increased to 2×10^7 compared to 1.5×10^6 (bottom) and 6.2×10^5 (top) in air and transconductance in dual-gate mode increased by about a factor of 2 compared to single-gate modes. This is because the average spatial separation between

charge carriers and the gate insulator is reduced. In single-gate devices, charge carriers are more highly confined, leading to enhanced interaction with interface. Interaction distance between charge carriers and interface in dual-gate devices becomes increased over singe-gate mode, leading to improved characteristics. Improved interface characteristics lead to improved S.S. and reduced Vth including increased on-current and on-off current ratio. It can also explain why the current density from a dual-gate device is larger than the sum of current densities of both top- and the bottom-gate devices, as shown in Figure 3.7 (b). Upon electric stressing, dual-gate operation resulted in greater stability than single-gate operations as shown in Figure 3.7 (c). This is also a consequence of the reduced interaction of charge carriers with the interfaces.



(a)

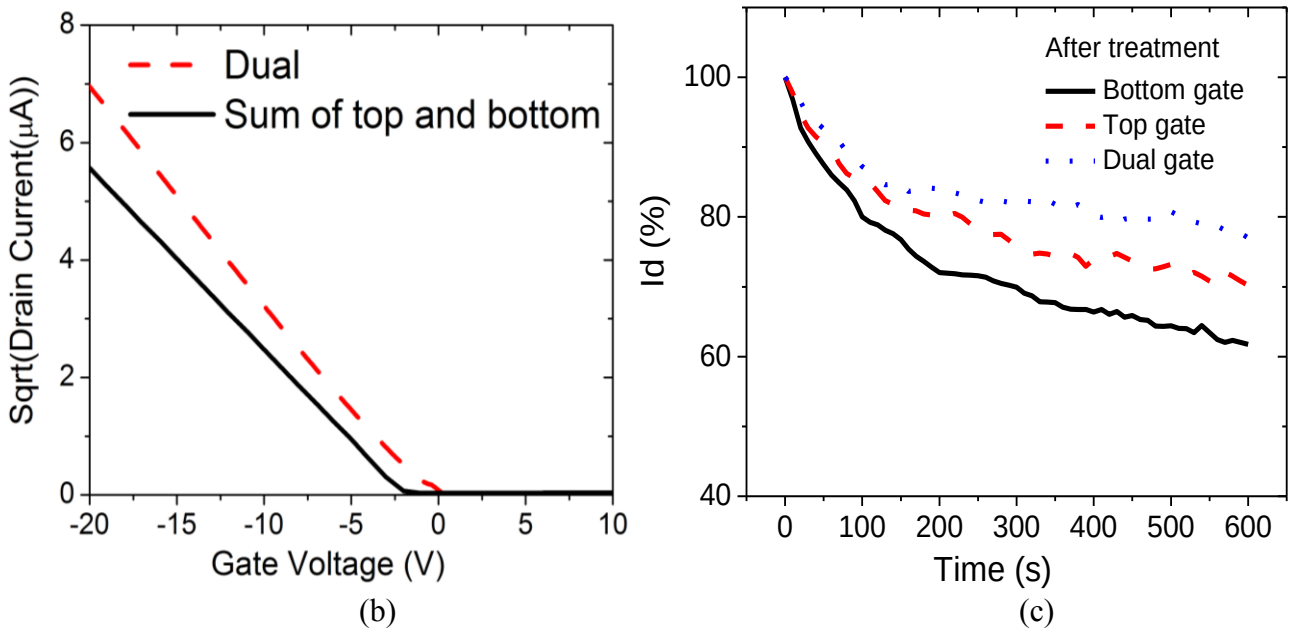


Figure 3.7 (a) The transfer characteristics in the top-gate, bottom-gate and dual-gate mode operations of a dual-gate PDPP-TNT TFT (b) the current density from a dual-gate device vs. the sum of current densities of both top- and the bottom-gate devices and (c) electrical stability in the top-gate, bottom-gate and dual-gate mode operations of a dual-gate PDPP-TNT TFT. Copyright 2011, American Institute of Physics

3.4 Charge carrier velocity distributions in high mobility diketopyrrolopyrrole-naphthalene copolymer TFTs

3.4.1 Experiments

Velocity distributions of charge carriers in PDPP-TNT TFTs have been obtained as follows. An input step-voltage from an HP 214B pulse voltage generator applied to the source electrode injects charge carriers into the channel. The time-dependent drain current is measured through a variable resistor (ranging from 50 kΩ to 1 kΩ), and yields

a distribution of arrival times of charge carriers at the drain electrode. Such measurements, while keeping the RC-time constant of the measurement circuit small, permit the extraction of velocity distributions of charge carriers [98-99].

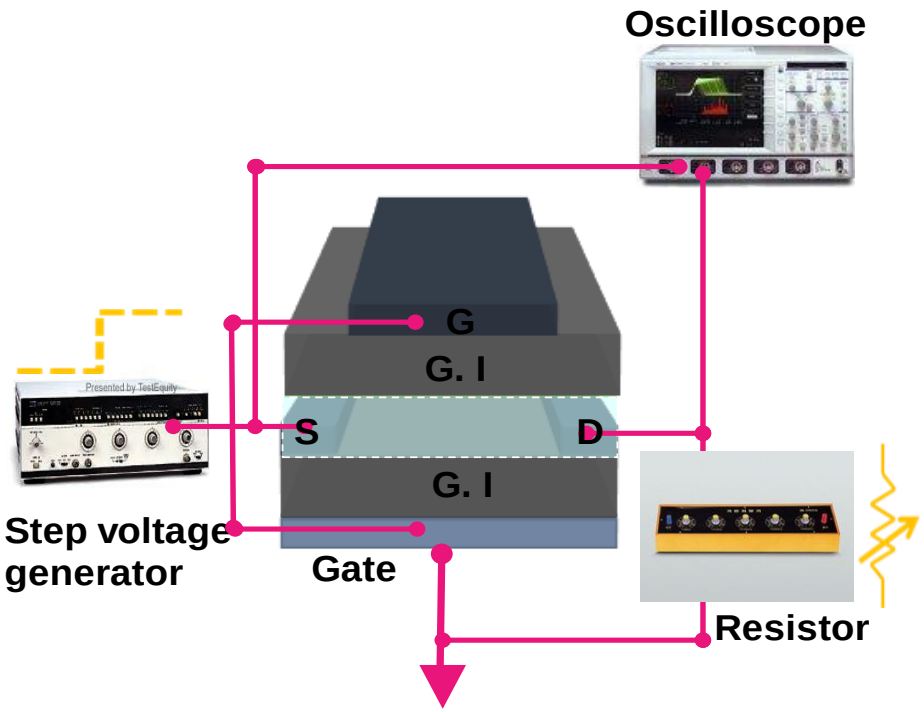


Figure 3.8 An illustration of time-domain measurement circuit using step voltage method

3.4.2 Results

The normalized transient drain current response as a function of drain resistance value has been plotted in Figure 3.9 (a). The 10 kΩ resistor represents the limiting value of drain resistance at which the overall dynamic response is not determined by the RC time constant of the measurement circuit for this particular experiment. The contact

resistance is not expected to be dominant in these experiments because the channel length was very long and a SAM treatment improved the electrical contact between the electrodes and the semiconductor. Figure 3.9 (b) shows that the normalized transient responses shift to shorter times as the step-voltage increases. The “turn-on time” is the time interval between the input signal of step-voltage and the point at which the normalized drain response is observable. The decrease in “turn-on time” with increasing source voltage means that effective mobility of the fastest charge carriers is becoming higher due to increased carrier concentration and lateral electric field [105-106] Figure 3.9 (c) shows the velocity distributions based on the arrival times of charge carriers at the drain electrode as a function of applied step-voltage. The velocity distribution was extracted by differentiating the normalized transient response and plotting as a function of velocity (defined as the channel length divided by the response time). As the step-voltage magnitude increases, the corresponding velocity distribution of charge carriers shifts to higher velocities, which shows that the velocity of charge carriers increases with lateral electric field.

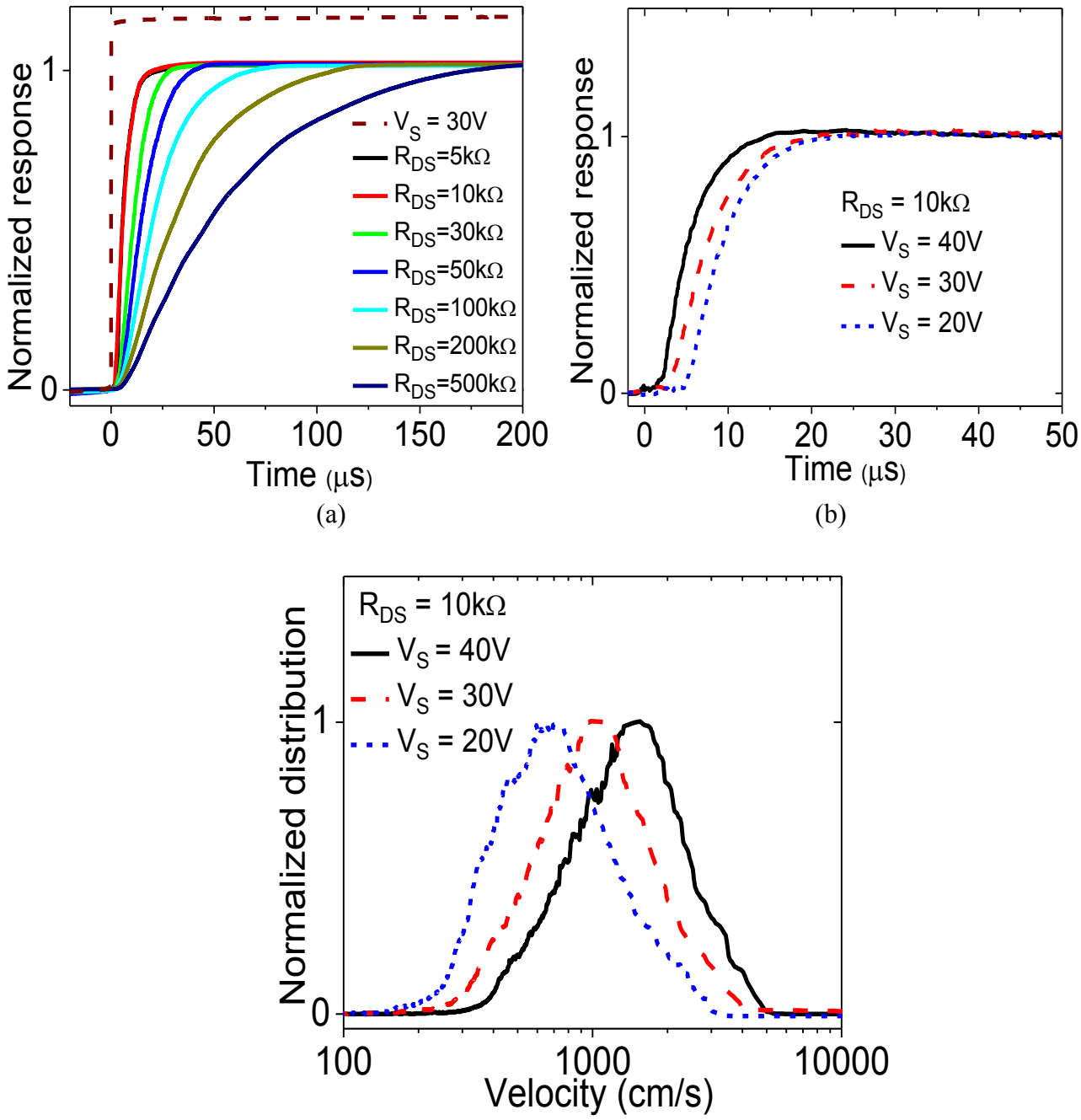


Figure 3.9 (a) The normalized transient response as a function of drain resistance value ranging from 5kΩ to 500kΩ and (b) the normalized transient response and (c) velocity distributions as a function of applied step-voltage ranging from 20V to 40V. Copyright 2012, American Institute of Physics

Time-domain transient measurements were performed on PDPP-TNT TFTs with different sample processing conditions. Glass transition temperature and liquid crystalline temperature are mainly related with the balance of aromatic and aliphatic moieties incorporated in polymer backbone. There is no liquid crystal transition and the choice of annealing temperatures was made to be in the typical range for conjugated polymer semiconductor. Figure 3.10 (a) shows the transfer characteristics of samples annealed at different temperatures. Samples annealed at 140 ºC possess a field-effect mobility of 0.4 cm^2/V-s extracted from DC measurements and samples annealed at 100 ºC possessed a mobility of 0.03 cm^2/V-s. Figure 3.10 (b) shows that in samples annealed at 100 ºC, the "turn-on time" and the time to reach quasi-equilibrium beyond the "turn-on time" takes much longer than in samples annealed at 140 ºC. It is also important to note that complicated dynamic response characteristics are observed in samples annealed at 100 ºC as opposed to samples annealed at 140 ºC. Very likely, there are regions of the device where the material organization is different from other areas, resulting in substantial differences in transit times of charge carriers. The velocity distribution in samples annealed at 100 ºC is broad and has two distinguishable peaks (A and B), whereas the room temperature charge carrier velocities are much greater and more tightly distributed in a single peak for samples annealed at 140 ºC, as shown in Figure 3.10 (c). Figure 3.10 (d) shows X-ray diffraction (XRD) results of PDPP-TNT TFTs with different annealing temperatures. The diffraction peak in samples annealed at 140 ºC is larger than that at 100ºC, indicating better crystallinity. When the annealing and XRD diffraction pattern for the polymer PDPP-TNT was correlated at various temperatures then it was found that, particularly at 140 ºC, the primary diffraction peak intensified with temperature compared to room temperature and 100 ºC as shown in Figure 3.10 (d).

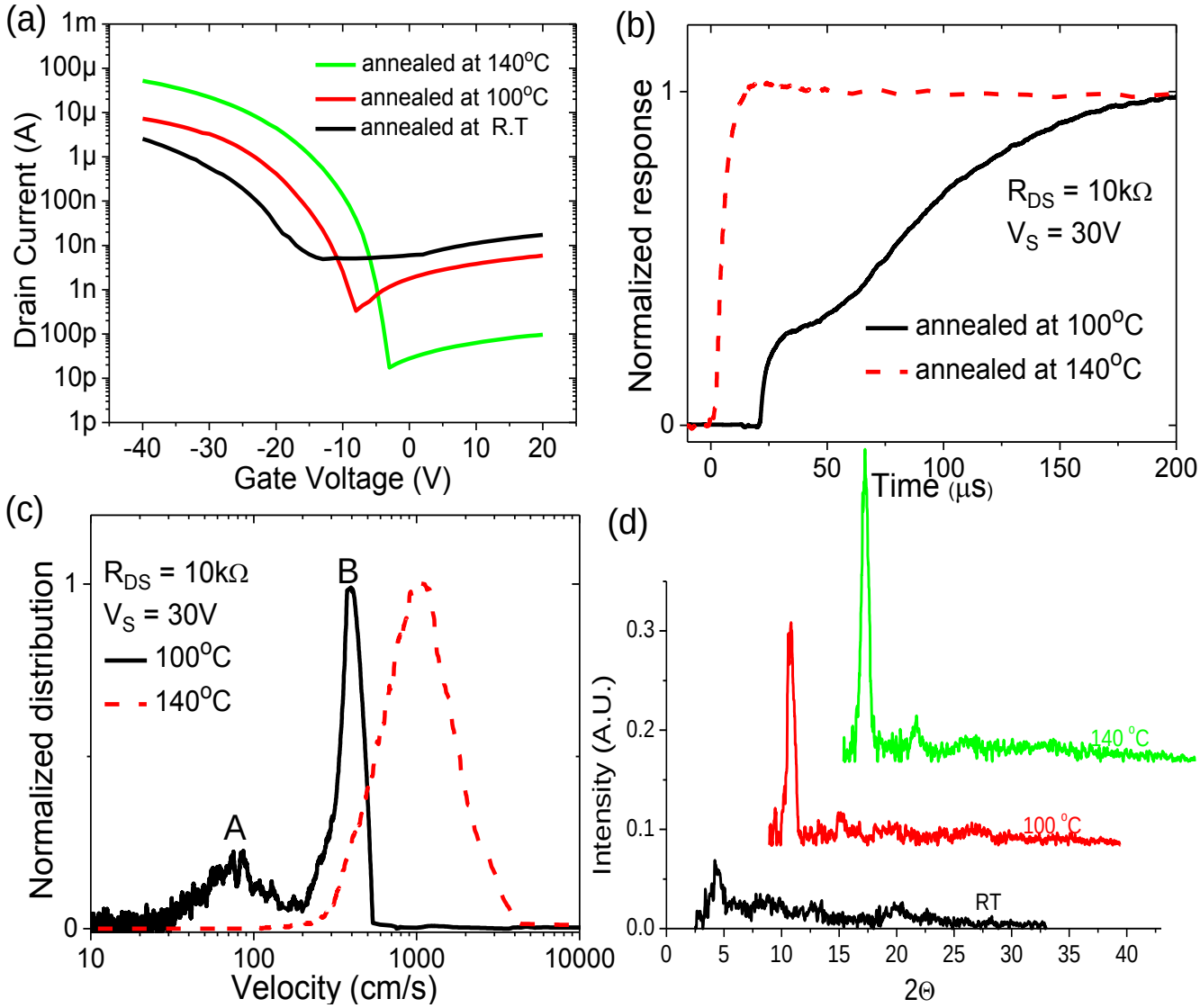


Figure 3.10 (a) The transfer characteristics of PDPP-TNT TFTs annealed at different temperatures (b) the normalized transient response and (c) velocity distributions on samples annealed at 100 ºC and 140 ºC (d) X-ray diffraction (XRD) PDPP-TNT semiconductor layers with different annealing temperatures. Copyright 2011, American Institute of Physics

It is known that post-deposition thermal annealing can improve the crystallinity of molecular ordering of the polymer thin films [107-108]. For the sample annealed at 140 ºC, the thermal motion of polymer chains could help chain packing into a higher degree of molecular ordering compared to at room temperature and 100 ºC, as shown in Figure 3.11. At the annealing temperature of 100 ºC, the 2-octyldodecyl side chains start to become softened and the layer-by-layer lamellar crystalline structure is partially formed. However, further enhancement in the temperature from 100 ºC to 140 ºC allows polymer chains mobile enough to self-assemble into more ordered crystalline structures and side chains allow the entire polymer chains to reorganize into more crystalline domains. The lower crystallinty at a lower annealing temperature for PDPP-TNT semiconductors can be explained by the lower softening temperature of the side chains of this polymer. At room temperature some polymeric chains are adopting face on orientation and some of them are adopting edge on orientation. After thermal annealing, there might be enhancement in edge on orientation population than the face-on orientation [109].

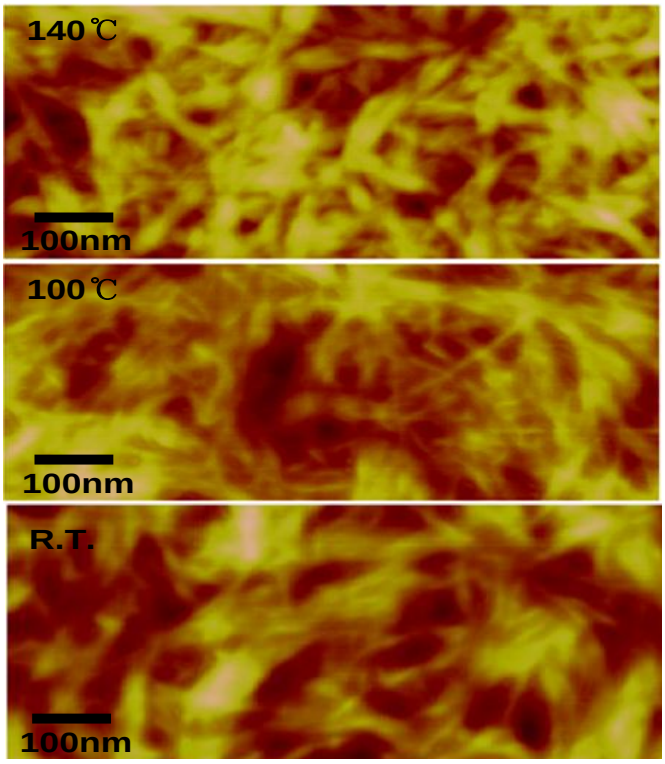


Figure 3.11 AFM images with different annealing temperatures

Temperature-dependent velocity distribution measurements were performed from 108 K to 300 K on PDPP-TNT TFTs annealed at 140 ºC. The device characteristics of PDPP-TNT TFTs were re-measured at room temperature after temperature cycling and were largely unchanged compared to the initial characteristics. Figure 3.12 (a) shows that the "turn-on time" and the time to reach quasi-equilibrium beyond the "turn-on time" become longer with decreasing temperatures. Furthermore, more complicated dynamic response characteristics are observed as measurement temperature decreases. Similar to results described above on samples which were annealed at 100 ºC, the velocity distributions shift to lower velocities and become bimodal with two distinguishable peaks at low measurement temperatures. We believe that the bimodal distribution observed in charge carrier velocity distribution measurements results from the inhomogeneity in the material

at the scale of the device dimension. Since these transistors possess a large ratio of channel width to channel length, various regions of the device might possess locally different morphologies. In such measurements on a large number of devices with different W/L, inhomogeneties were found to a larger degree in large W/L samples than smaller ones, which supports our view as shown in Figure 3.12 (c) The enhanced occurrence of bimodal distributions at low temperatures and in samples annealed at 100 ºC suggests that inhomogeneities manifest in a more pronounced manner under these conditions or in these samples. Going a step deeper, a possible reason for this inhomogeneity is that the trap distributions are spatially non-uniform and that this shows up as a bimodal velocity distribution. This effect appears to be more pronounced at lower measurement temperatures. Another possible reason is contacts: contacts and the traps in the semiconductor (which influence carrier injection) in the vicinity of the contacts can also be inhomogenous. Such trap distributions influence carrier injection from the contact and the magnitude of current measured. It does not correlate to bias stress. It may be related to crystalline and amorphous regions. The two peaks coalesce to form a single peak at high measurement temperatures, close to room temperature as shown in figure 3.12 (b). These results indicate that transport is more inhomogeneous in PDPP-TNT TFTs at low measurement temperatures.

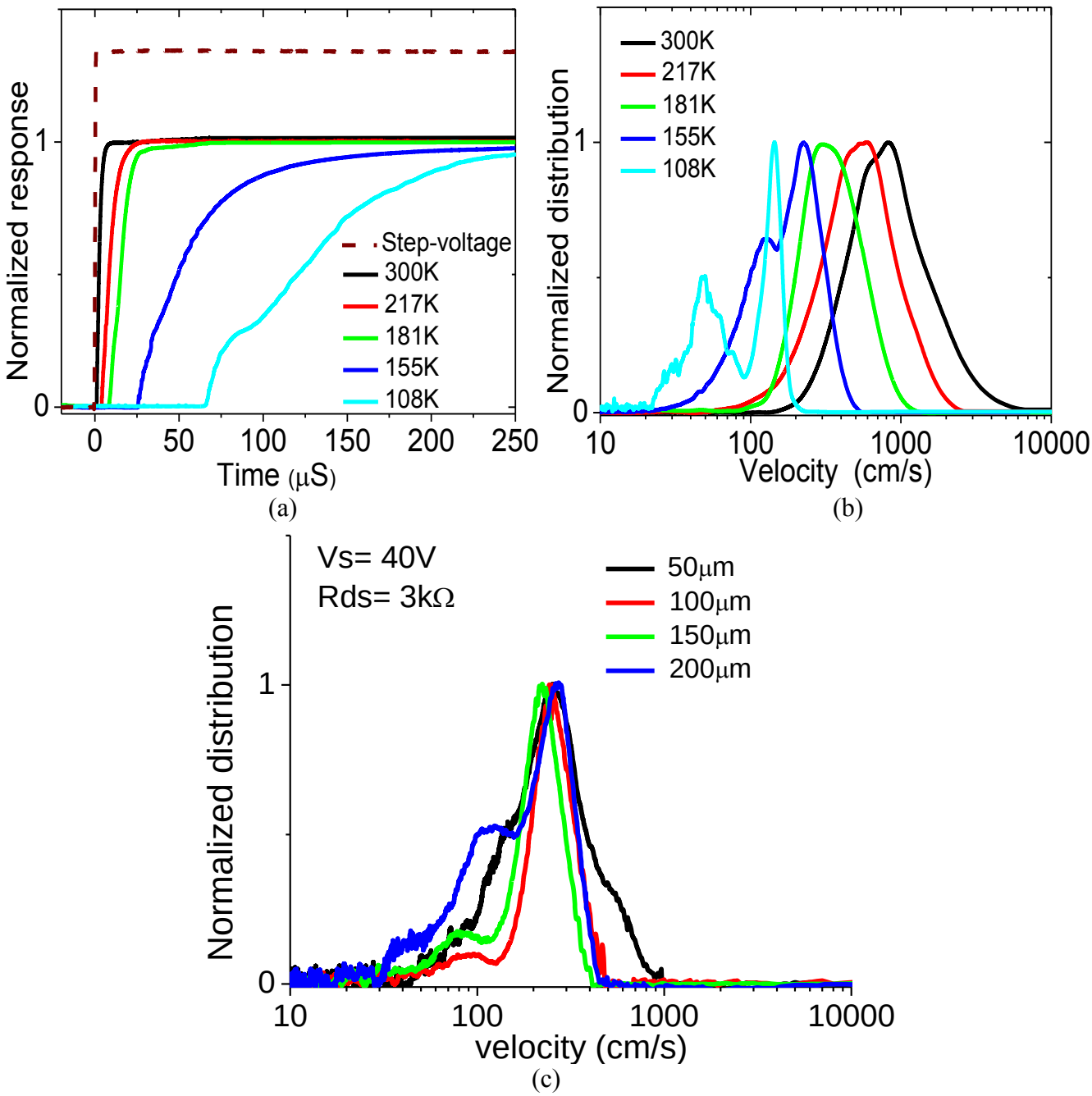


Figure 3.12 Temperature-dependent measurements from 108 K to 300 K on PDPP-TNT TFTs annealed at 140 ºC: (a) the normalized transient response (b) velocity distributions of charge carriers and (c) velocity distributions of charge carriers with different channel lengths. Copyright 2011, American Institute of Physics

3.5 Charge transport measurements in steady-state and under non-quasi-static conditions in diketopyrrolopyrrole-naphthalene copolymer TFTs

3.5.1 Experiments

Temperature-dependent field-effect mobility measurements were performed from 98 K to 300 K with bottom- and top-gate operations in PDPP-TNT TFTs. The device characteristics were re-measured at room temperature after temperature cycling and were almost unchanged compared to initial characteristics. It means that the physical and material properties of PDPP-TNT TFTs were not substantially altered by the temperature cycling.

3.5.2 Results

Figure 3.13 shows the results obtained by temperature-dependent field-effect mobility measurements with bottom- and top-gate operations. The plots show the linear field-effect mobility as a function of gate voltage as well as temperature. The field-effect mobilities decreased with temperature as well as increased with applied gate voltage in both bottom- and top-gate operation.

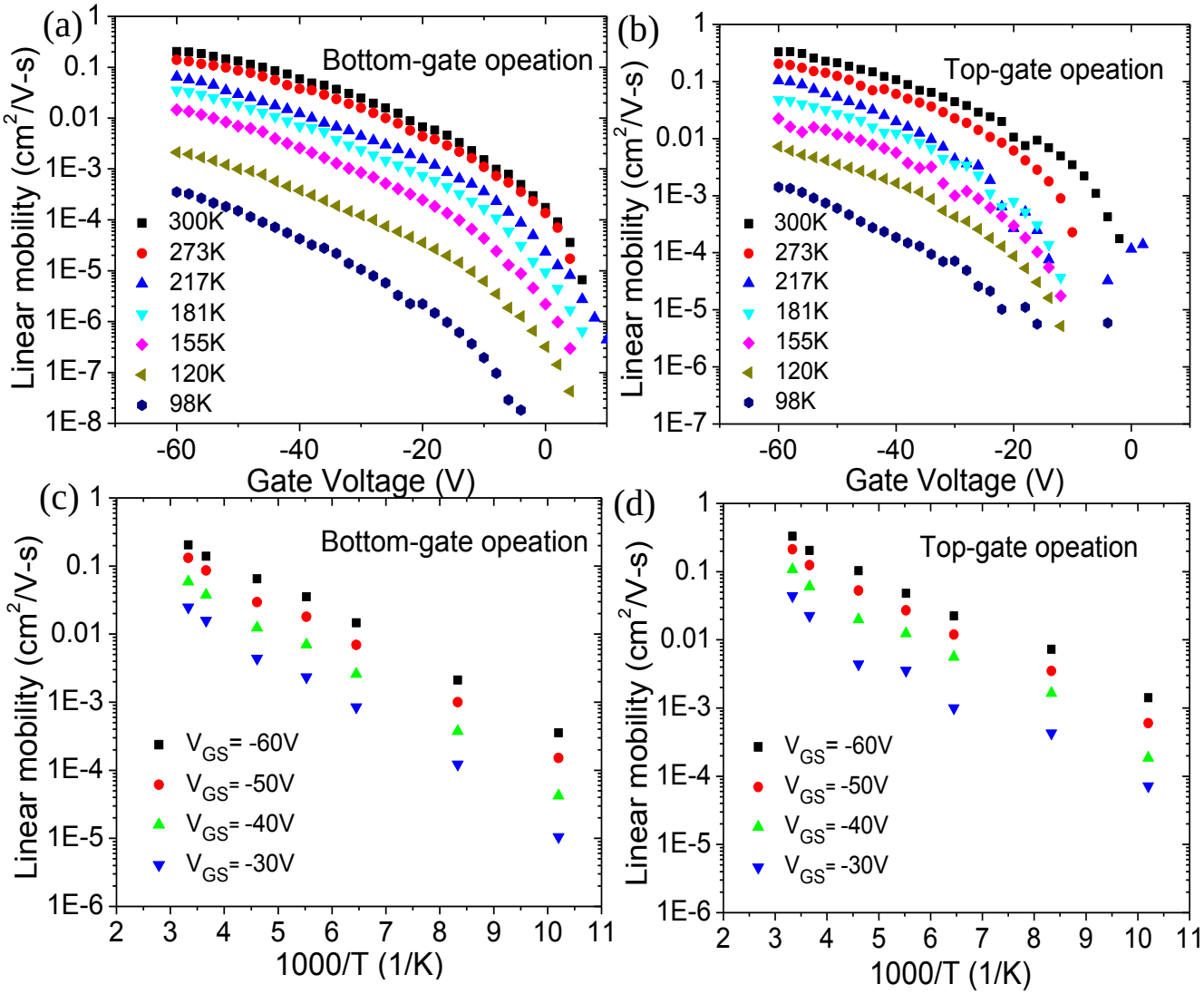


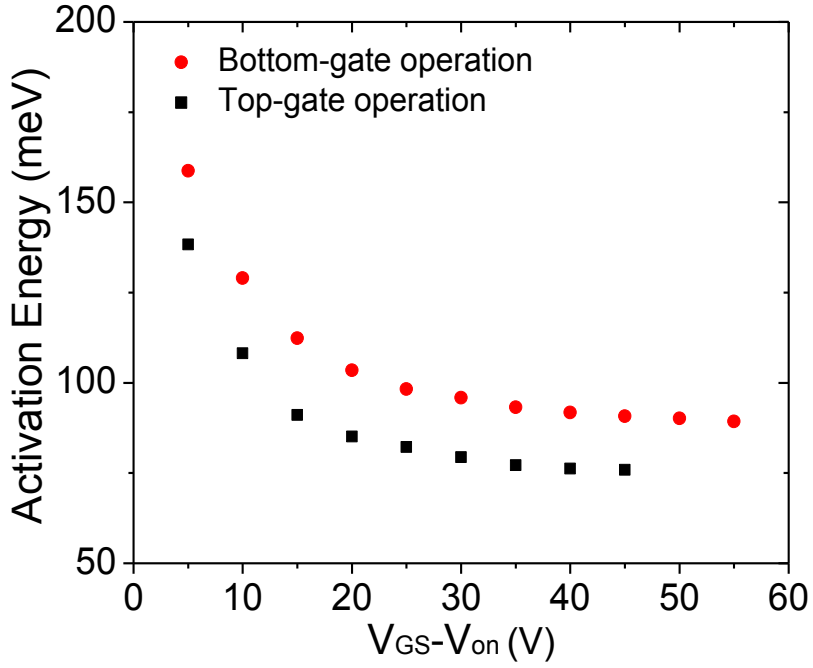
Figure 3.13 Temperature-dependent field-effect mobility measurements from 98 K to 300 K on PDPP-TNT TFTs

Figure 3.14 (a) shows the plot of activation energy versus V_{GS}-V_{ON} in bottom- and top-gate operations. V_{ON} is the turn-on voltage of the device at which significant carrier accumulation is observed. Activation energies are extracted from the slope by fitting the data with the above equation. The activation energy decreases with increasing

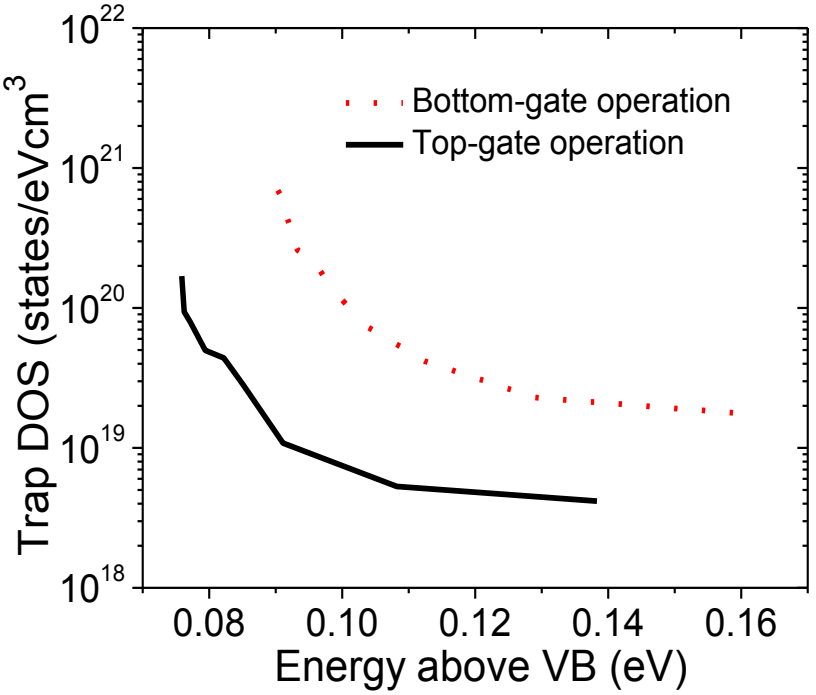
V_{GS}-V_{ON} in both bottom- and top-gate operations. This decrease in activation energy fits the MTR model of charge transport, particularly for low values of gate voltage [32]. Significantly, the activation energy measured under top-gate operation is less than that under bottom-gate operation. The activation energy roughly corresponds to the energy distance from occupied trap states to the transport level [32]. Figure 3.14 (b) shows the density of trap states (trap DOS) in the band gap of PDPP-TNT TFTs as calculated by Lang method as following [110]:

$$N(E) = \frac{C_i}{qA}\left[\frac{\partial E_A}{\partial V_G}\right]^{-1}$$

where C_i is capacitance of gate dielectric, A is gate-voltage-independent effective accumulation-layer thickness, V_G is applied gate voltage and L is the thickness of gate dielectric. The trap DOS calculated from top-gate operation is less than that from bottom-gate operation. The result supports the picture that the better device performance in top-gate operation with polymeric gate dielectric is related to the lower trap DOS.



(a)



(b)

Figure 3.14 (a) Activation energy with a function of V_{GS}-V_{ON} and (b) the density of trap states as calculated by Lang method in bottom- and top-gate operations

Figure 3.15 (a) shows the normalized transient drain current response as a function of drain resistance value. When the drain resistance is less than 5 kΩ, the dynamic response is no longer a function of drain resistance. Figure 3.15 (b) shows normalized transient drain current response in top-, bottom- and dual-gate operations. The normalized transient responses in dual-gate operation shift to shorter "turn-on time" than in single-gate operation, as shown in Figure 3.15 (b). The decrease in "turn-on time" in dual-gate mode means that effective mobilities become higher compared to single-gate mode. Furthermore, the time to reach quasi equilibrium in dual-gate operation is less than in single-gate operation.

The results confirm that the corresponding velocity distribution of charge carriers in dual-gate operation shifts to higher velocities than in single-gate operation, as shown in Figure 3.15 (c). It is also noted that dual-gate operation exhibits fewer low velocity carriers compared to single-gate operation as indicated by the shaded region in Figure 3.15 (c). Overall, higher velocity carriers in dual-gate operation can improve the frequency response of the FETs, which can result in better image quality and energy efficiency in display applications. The velocity distributions of charge carriers measured under dual-gate operation is not a simple superposition of the velocity distributions of top- and bottom-gate operation modes. It means that the dual-gate configuration influences the charge carrier transport and velocity distributions. The location of the charges in the channel with respect to the gate insulator interface has a significant impact on trapping and field-effect mobility. In dual-gate devices the charges move, on average,

further away from the insulator interface. This will impact the extent of trapping and be reflected in the velocity distribution.

There have been discussions that improved device performance of sub- and above-threshold regions in dual-gate TFTs results from increased capacitance of gate insulator. The value of the total gate capacitance in dual-gate operation becomes increased due to the parallel connection of both top- and bottom-gate dielectrics. Figure 3.15 (d) shows the charge carrier velocity distributions in single-gate with a 160 nm (which is assumed to possess same capacitance of gate dielectric as dual-gate) and a 200nm thick SiO_2 compared to dual-gate. Dual-gate operation exhibits increased carrier velocity compared to single-gate with same capacitance. The result means that improved dual-gate characteristics cannot be entirely attributed to the increased carrier density in due to the larger value of capacitance. Rather, it is the reduction in the number of low velocity carriers seen in dual-gate devices that is principally responsible for the improved performance. We have clearly demonstrated this effect for the first time in a thin-film transistor.

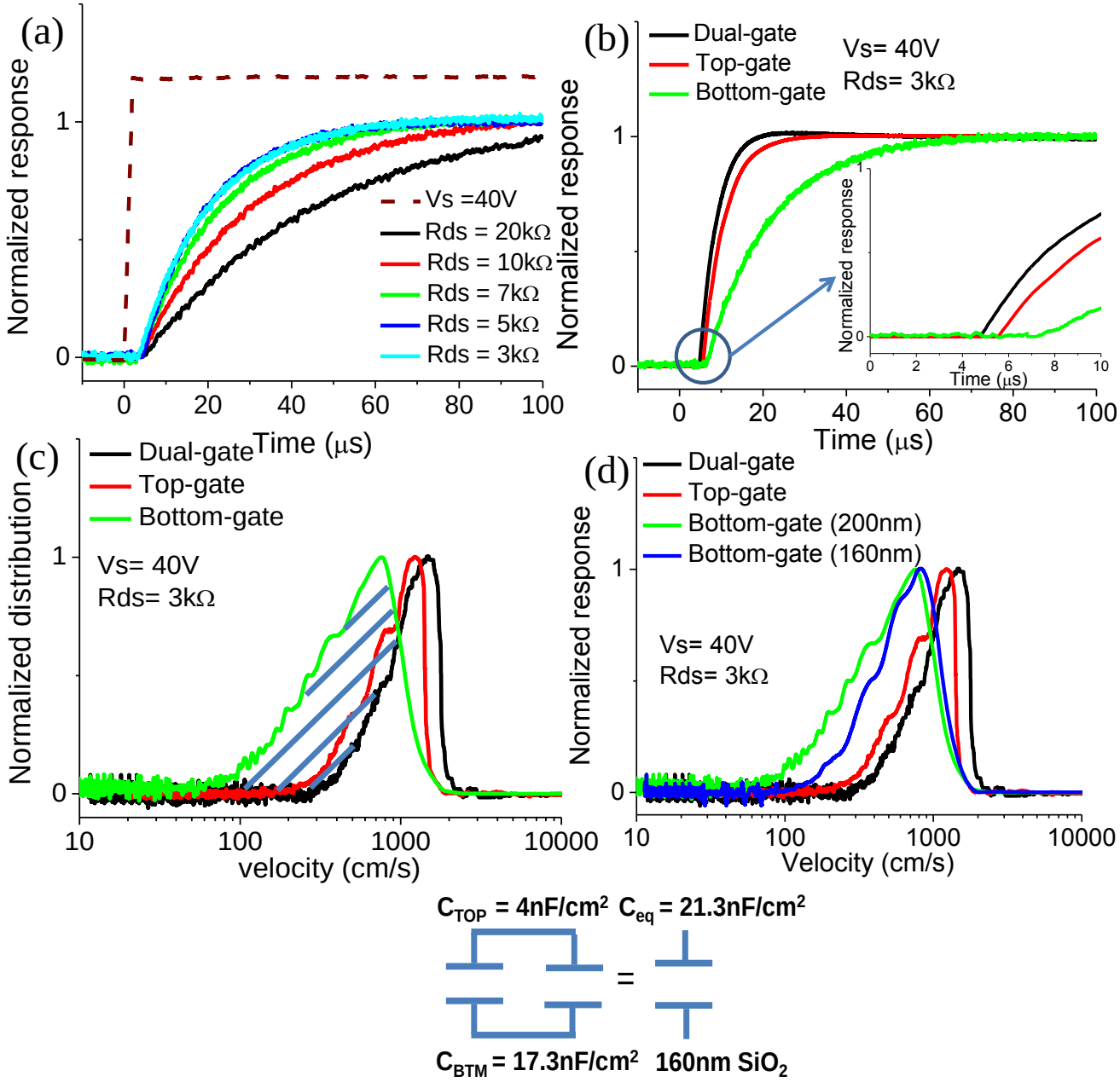


Figure 3.15 (a) Normalized transient response as a function of drain resistance values (b) normalized transient response (c) corresponding velocity distributions of charge carriers in top-, bottom- and dual-gate operation and (d) The effect of capacitance value on velocity distributions in PDPP-TNT TFTs. Copyright 2012. IEEE

3.6 Conclusions

Top-gate TFTs with the polymer PDPP-TNT with optimized mobilities of ~1 cm^2/V-s was investigated. This requires the use of suitable surface treatments and a polymer gate insulator. In addition, we have investigated dual-gate TFTs, which possess higher drive currents and improved gate control over single-gate TFTs. Dual-gate TFTs also exhibit increased transconductance, reduced Vth, improved S.S. and increased on-off current ratio compared to single-gate architectures. The improved performance of dual-gate devices is a result of reduced interaction between the charge carriers and the insulator interfaces. The velocity distribution of charge carriers in high mobility PDPP-TNT TFTs using transient measurements was also measured. Processing conditions such as annealing temperature influence velocity distributions and 100 ºC anneals result in inhomogeneous charge carrier transport at room temperature. The velocity distribution becomes very inhomogenous at low measurement temperatures even in samples annealed at relatively high temperatures (140 ºC). Temperature-dependent velocity distributions can provide additional information to understand charge carrier transport, which is not possible to obtain from steady-state transport measurements. Charge transport measurements in steady-state and under non-quasi-static conditions reveal that this improved performance is a result of a smaller fraction of charge carriers that move through slow trap states. The mobility of the fastest carriers is increased in dual-gate devices. We also compare the activation energies for charge transport in the top-gate and bottom-gate configurations. Top-gate TFTs with the polymer PDPP-TNT with optimized mobilities of ~1 cm^2/V-s was investigated. This requires the use of suitable

surface treatments and a polymer gate insulator. In addition, we have investigated dual-gate TFTs, which possess higher drive currents and improved gate control over single-gate TFTs. Dual-gate TFTs also exhibit increased transconductance, reduced Vth, improved S.S. and increased on-off current ratio compared to single-gate architectures. The improved performance of dual-gate devices is a result of reduced interaction between the charge carriers and the insulator interfaces. The velocity distribution of charge carriers in high mobility PDPP-TNT TFTs using transient measurements was also measured. Processing conditions such as annealing temperature influence velocity distributions and 100 ºC anneals result in inhomogeneous charge carrier transport at room temperature. The velocity distribution becomes very inhomogenous at low measurement temperatures even in samples annealed at relatively high temperatures (140 ºC). Temperature-dependent velocity distributions can provide additional information to understand charge carrier transport, which is not possible to obtain from steady-state transport measurements. Charge transport measurements in steady-state and under non-quasi-static conditions reveal that this improved performance is a result of a smaller fraction of charge carriers that move through slow trap states. The mobility of the fastest carriers is increased in dual-gate devices. We also compare the activation energies for charge transport in the top-gate and bottom-gate configurations.

CHAPTER 4 DEVICE PHYSICS OF POLYMER FIELD-EFFECT TRANSISTORS BASED ON DIKETOPYRROLOPYRROLE-BENZOTHIADIAZOLE COPOLYMER

4.1 Introduction

Most organic and polymeric semiconductors, when employed as active materials in FETs, result in substantially unipolar device operation [111-112]. The main reason for this is that one of the carrier species gets trapped in states usually present at the semiconductor-dielectric interface and in the gate insulator. Careful choice of the dielectric (to suppress trapping) or coating of the dielectric surface with a suitable self-assembled monolayer (SAM), mitigate such trapping effects. Ambipolar semiconductors, which transport both electrons and holes with similar mobilities, are useful for various applications ranging from light-emitting devices to the logic circuits [113-114]. In applications employing ambipolar transistors as circuit elements, enhanced p-channel or n-channel behavior can be achieved through the use of contact modification methods [111]. It therefore represents an alternative to using two separate semiconductors for n-FETs and p-FETs.

We recently reported design and synthesis of a new ambipolar polymeric semiconductor based on diketopyrrolopyrrole-benzothiadiazole copolymer (PDPP -TBT) [109, 115]. This semiconductor possesses balanced electron and hole mobilities of ~0.5 cm^2/V-s in TFT devices with symmetric source and drain gold electrodes in top contact/bottom gate device geometry. The higher electron and hole mobilities observed in this material are due to a number of favorable factors. In this chapter, we explore several

device configurations using this semiconductor including top-gate and dual-gate architectures. We have obtained the highest electron and hole mobilities (both in excess of 0.5 cm^2/V-s) attained in a single organic semiconductor. This has been achieved without the use of special dielectrics that suppress electron trapping [113, 116]. We report the effect of various surface treatments on electron and hole injection from gold source and drain contacts. We also discuss sub-threshold conduction and its dependence on the gate (top vs bottom vs dual gate). We report on the measurement of the electron and hole velocity distributions in this semiconductor.

Previous reports on high mobility ambipolar semiconductor FETs (both thin-film and single crystal) have not achieved such a high minimum carrier mobility value [117-119]. In some cases, one of the carrier mobilities is quite high (for example, the hole mobility in Ref. [117] is 1.64 cm^2/V-s, but the electron mobility is only 0.17 cm^2/V-s.

Significantly, there have been no prior studies on charge transport and the trap DOS for both electrons and holes in such high mobility ambipolar organic semiconductors [120-121]. In order to understand the charge transport behavior of this unique material (PDPP-TBT) which has high mobilities and balanced ambipolar charge transport in OTFT devices, the activation energy has been measured as a function of gate bias (or induced carrier concentration) at various temperatures in the range 120 K to 300 K. We have also calculated the trap DOS in ambipolar PDPP-TBT TFTs based on activation energy as a function of gate voltages using two analytical methods following the approach by Lang *et al*. and Kalb and Batlogg.

4.2 Diketopyrrolopyrrole-benzothiadiazole copolymer

In the following, a brief description of the synthesis of the polymer is provided after the more detailed description published by Dr. Prashant Sonar *et al*., who provided the material [115]. In a Schlenk fl ask 3,6-bis-(5-bromothiophen-2-yl)-N , N′-bis((octyldodecyl)-1,4-dioxo-pyrrolo[3,4-c]pyrrole (0.300 g, 0.29 mM), 4,7-bis(4,4,5,5-tetramethyl-1,3,2-dioxabrolan-2-yl) benzothiadiazole (0.114 g, 0.29 mM), 2M aqueous K_2CO_3 solution (3 mL), and 2 drops of N -methyl- N , N -dioctyloctan-1-ammonium chloride (Aliquat 336) were dissolved in toluene (6 mL) [115]. The solution was purged with Argon for 30 min, and tetrakis(triphenylphosphine) palladium (20 mg, 0.017 mM) was added. The reaction was stirred at 80 ° C for 3 days. Then a toluene solution of phenyl boronic acid was added and the mixture was stirred for an additional 4 hours, followed by the addition of a few drops of bromobenzene, after which it was stirred overnight. The resulting mixture was poured into a mixture of methanol and water and stirred overnight. The dark precipitate was re-dissolved in chloroform and added to methanol (250 mL). The resulting solid was filtered off and subjected to Soxhlet extraction for 2 days successively in methanol, acetone, and hexane for the removal of oligomers and catalytic impurities. The remaining polymer was extracted with chloroform and precipitated again from methanol, filtered, washed with methanol, and dried under vacuum at room temperature. (0.200 g, 69% yield). Mw/ Mn (GPC) = 42 400/ 60 200.

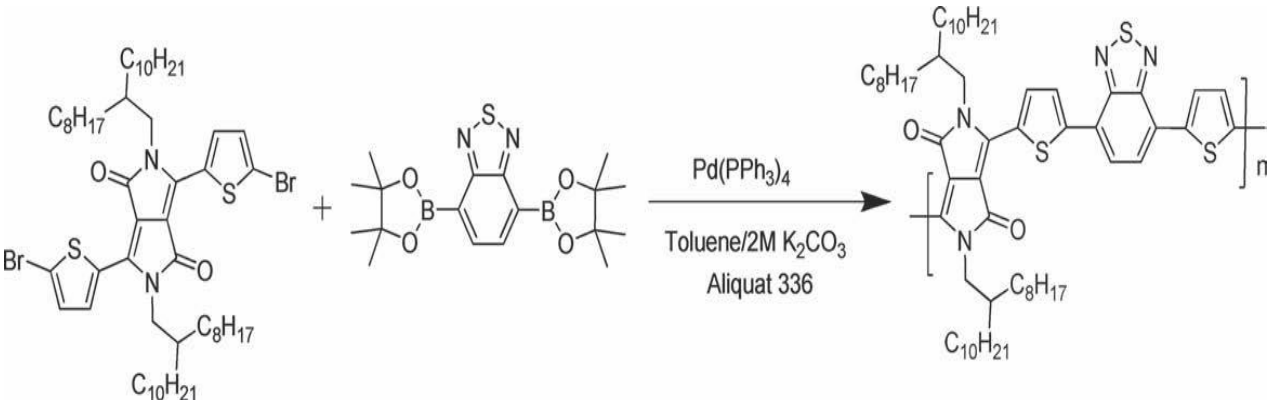


Figure 4.1 Synthesis of PDPP-TBT [From 115]

The combination of the DPP moiety with a donor-acceptor-donor (D-A-D) building block, thiophene-benzothiadiazole-thiophene (TBT) was done deliberately to form a copolymer with a repeat unit of DPP-TBT and design for balanced hole- and electron-transport properties. Furthermore, fused-ring aromatic structures tend to form π –π stacks with a large overlap area which is favorable for charge transport. The higher electron and hole mobilities observed in this material are due to a number of favorable factors. First, the energy levels of the π* and π bands (which correspond to the conduction band and valence bands) are about 4.0 eV and 5.2 eV. These energy levels ameliorate the extent of trapping of both holes and electrons, permitting the facile movement of both types of charge carriers. This relatively low band-gap is itself due to the combination of donor-acceptor blocks in the conjugated backbone. If the LUMO level is < 4.0 eV then deep trap states caused by moisture, oxygen and other impurities compete for electrons. If the HOMO is much less than 5.2 eV the material is easily oxidized leading to high off-currents [120-121].

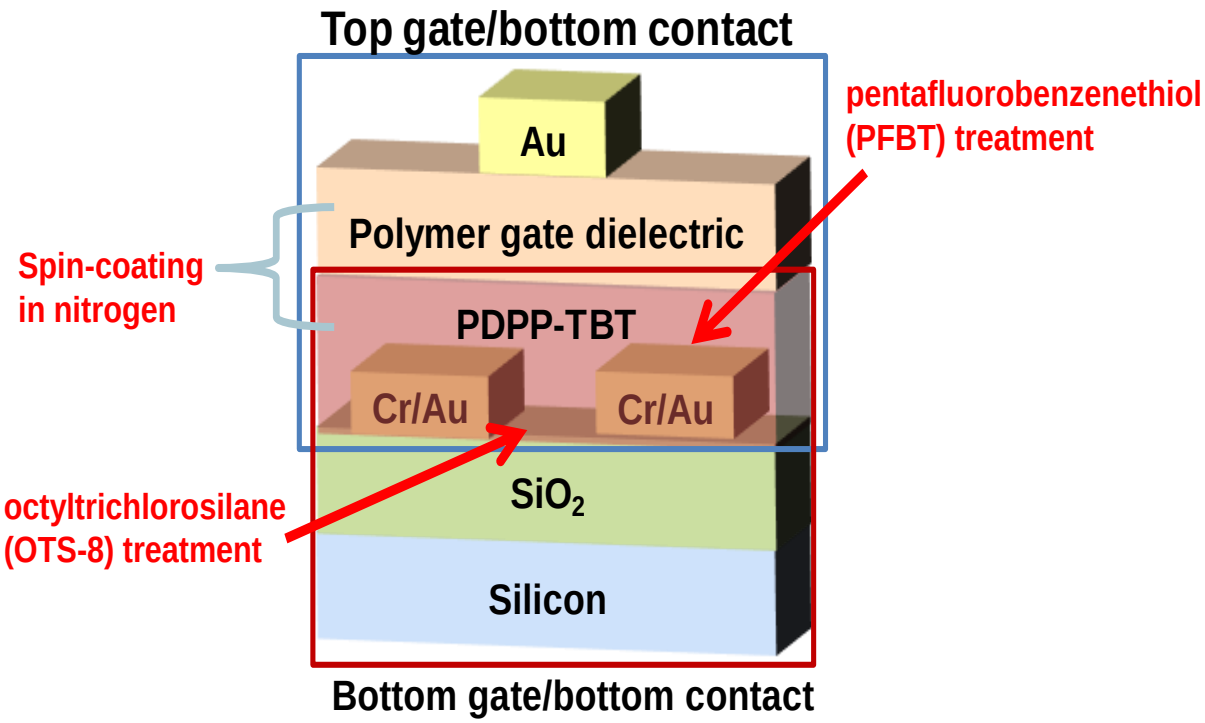
4.3 Characteristics of high-performance ambipolar organic FETs based on diketopyrrolopyrrole-benzothiadiazole copolymer

4.3.1 EXPERIMENTS

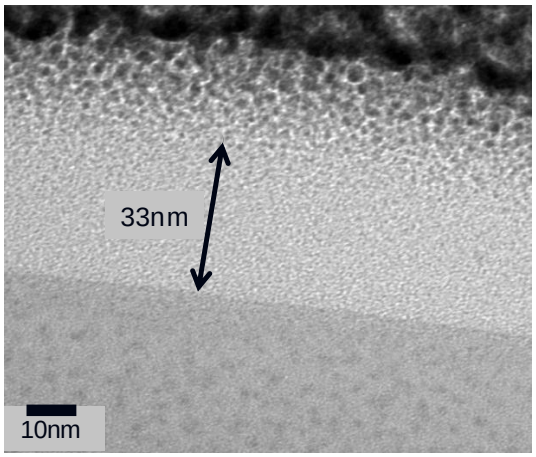
Figure 4.2 (a) shows the schematic cross-section of a dual-gate ambipolar polymer TFT based on PDPP-TBT. Device fabrication started with a 1-10 Ω-cm silicon substrate, also used as the bottom-gate electrode. This silicon substrate is thermally oxidized to resulting in a 200 nm thick silicon dioxide layer which is subsequently treated with UV ozone for 5 minutes. Following this step, a 47.5 nm thick chrome/gold (2.5 nm/45 nm) bi-layer source and drain electrodes were deposited by thermal evaporation. In order to reduce the contact resistance between the source/drain metal and the PDPP-TBT semiconductor, gold electrodes were surface-treated with a SAM of pentafluorobenzenethiol (PFBT) and NBT. The samples were immersed into a dilute PFBT (NBT) solution in isopropyl alcohol (10 mM) for 1 hour, then rinsed with pure isopropyl alcohol to remove the residual PFBT (NBT), and then annealed at 120 ºC for 30 minutes. In addition, the samples were exposed to OTS-8 vapor at 110 ºC for 6 hours and then treated with isopropyl alcohol. Both PFBT and OTS-8 treatment were performed under an inert atmosphere.

The PDPP-TBT solution was formed using chloroform as the solvent (7 mg/mL concentration) with magnetic stirring at 53 ºC for 6 hours in an inert environment. The semiconductor film was formed by spin-coating for 40 seconds at 1600 rpm, followed by pre-annealing at 200 ºC for 30 minutes. Figure 4.2 (b) shows the transmission electron

micrograph (TEM) of an OTS-8-treated bottom-gate device with a 33 nm thick PDPP-TBT semiconductor layer.



(a)



(b)

Figure 4.2 (a) the schematic cross-section of a dual-gate polymer TFT based on PDPP-TBT and (b) TEM image of OTS-8-treated bottom gate/bottom contact device. Copyright 2012. IEEE

Top gate and dual-gate devices employ as-supplied polymeric dielectric (D139) as the top-gate insulator. The capacitance value for the top gate insulator is ~ 4 nF/cm^2. Finally, a 45 nm thick gold top-gate electrode was deposited by thermal evaporation. The device fabrication was completed with thermal annealing at 140 ºC for 10 hours. Both the spin-coating and thermal annealing of the PDPP-TBT and D139 layers were performed in a nitrogen box. The PDPP-TBT TFTs possess a channel width of 1000 μm and a channel length of 50 μm. All measurements were performed in a Desert Cyrogenics vacuum prove station with a pressure lower than 10^{-3} Torr.

4.3.2 RESULTS

Figure 4.3 (a) and (b) show the output and the transfer characteristics of a top-gate TFT based on PDPP-TBT operating in electron- and hole-enhancement modes, respectively. At low negative gate voltages ($|VG| < 20$) in the hole-enhancement mode, the drain current increases with decreasing gate voltage and does not saturate but instead increases non-linearly with drain voltage. This is a result of electron injection from the drain electrode [122-125]. Similarly, at low positive gate voltage ($VG < 10$) in the electron-enhancement mode, a non-saturating current with increasing drain voltage and decreasing gate voltage is observed. This characteristic is due to hole injection from the drain electrode. At higher gate voltages, linear and saturation regions, expected for a field-effect transistor operation in accumulation mode, are clearly observed. Similar behavior has been observed in ambipolar TFTs reported by several groups [122-125].

The transfer characteristics show good electrical performance with on-off current ratios as high as 10^4 with 0.91 V/decade of S.S, as shown in Figure 4.3 (b). Optimized top-gate PDPP-TBT TFTs possess gate leakage current lower than 1nA. Due to the combined effects of OTS-8 and PFBT surface treatments, samples annealed under optimized conditions possess a hole mobility of 0.53 cm^2/V-s and an electron mobility of 0.58 cm^2/V-s, as shown in Figure 4.3 (c).

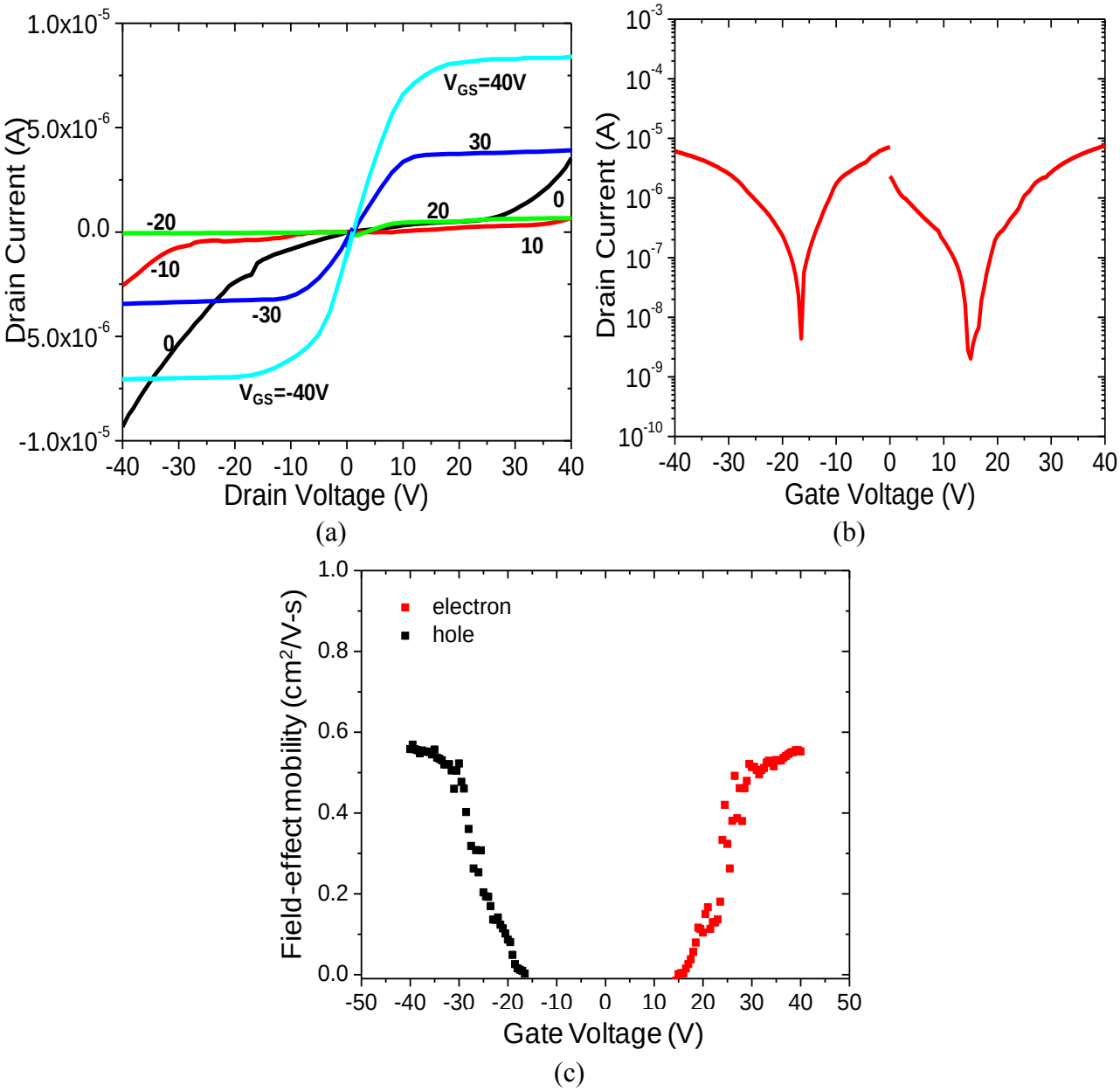


Figure 4.3 (a) The output characteristics, (b) the transfer characteristics and (C) the saturation field-effect mobility vs. gate bias of top-gate PDPP-TBT TFT operating in electron-enhancement and hole-enhancement modes. Copyright 2012. IEEE

It has been reported that the SAM treatment plays a crucial role in increasing molecular ordering by modifying the surface energy at the semiconductor-insulator interface, which results in better charge carrier injection and transport [126-127]. In addition, thermal post-annealing has been reported to improve molecular ordering of many polymeric semiconductors [128-129]. As shown in Figure 4.4, through the use of such surface treatments and thermal annealing, the mobility of electrons and holes increased from 0.18 cm^2/V-s to 0.58 cm2/V-s and from 0.24 cm^2/V-s to 0.53 cm^2/V-s respectively. In addition, the Vth of electrons and holes decreased from 34.5 V to 15.8 V and from -33.7 V to -17.1 V, respectively. Significantly, non-uniformity in device characteristics was reduced by thermal post-annealing. Similar behavior has also been reported previously in other materials [130].

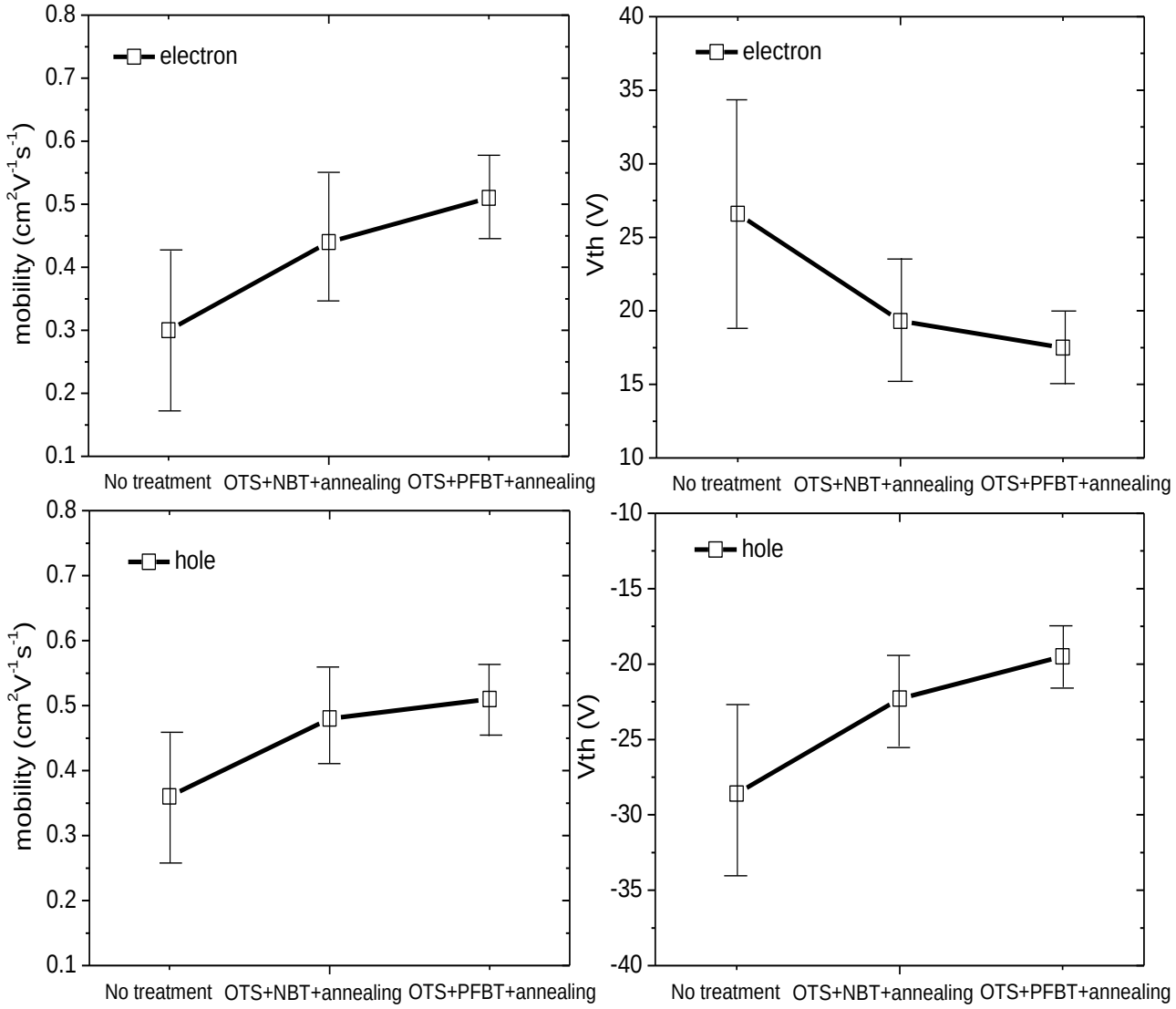


Figure 4.4 Comparisons of the mobility and the threshold voltage in electron-enhancement and hole-enhancement modes of non-treated, OTS+NBT+annealed and OTS+PFBT+annealed top-gate PDPP-TBT TFTs. Copyright 2012. IEEE

The inverse of slope of the output characteristics in linear region close to Vds ≈ 0V are compared for non-surface treated and surface treated samples and the data are shown in Figure 4.5. This clearly indicates the improvement in electrical contact between the source/drain metal electrodes and the PDPP-TBT semiconductor layer.

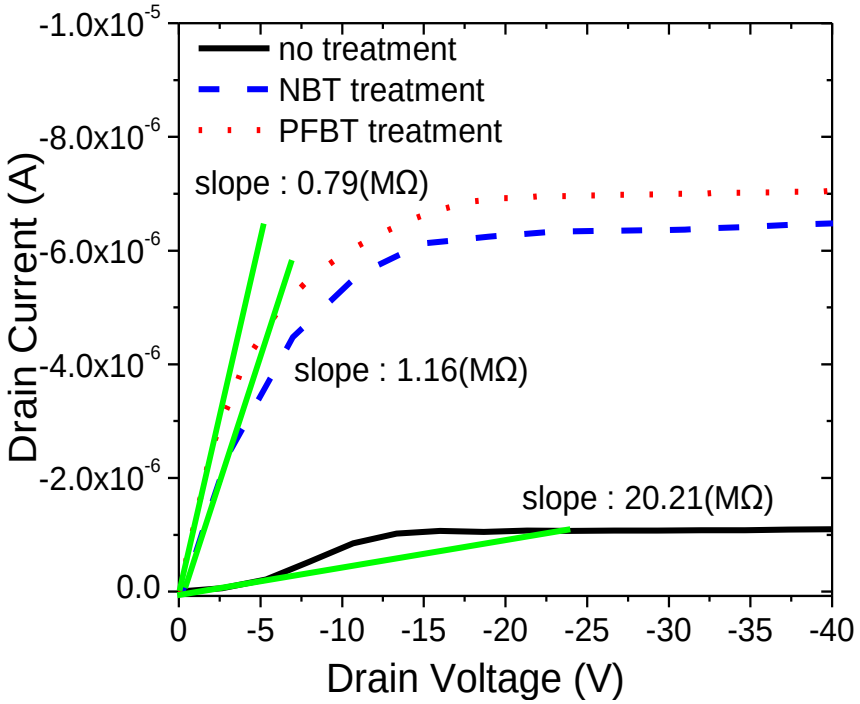


Figure 4.5 The effect of SAMs treatment on electrical contact of PDPP-TBT TFTs, which is extracted by the slope from the output characteristics in linear region at Vds ≈ 0V

As shown in Figure 4.6, dual-gate ambipolar PDPP-TBT TFTs have increased on-currents, lower Vth and improved S.S. and leakage currents compared to a top-gate or a bottom-gate device. Furthermore, improved saturation behavior is also observed. These results can be also explained by the reduced average spatial separation between charge carriers and the gate insulator as mentioned in previous chapter. In addition, the decreased Vth in the dual-gate structure increases |Vgs – Vth|. As a result of this, the non-

saturating current caused by minority charge injection from the drain region in ambipolar organic FETs is decreased. As a consequence of the effects discussed above, the current density from a dual-gate structure should be larger than the sum of both top- and the bottom-gate structures. The inset in Figure 4.6 shows the square root of drain current vs. gate voltage in PDPP-TBT TFTs. The drain current obtained from the dual-gate mode operation is larger than the sum of two drain currents obtained from single-gate mode operations. It is consistent with the results that the transconductance value of a dual-gate device is larger than that sum transconductances of single-gate devices.

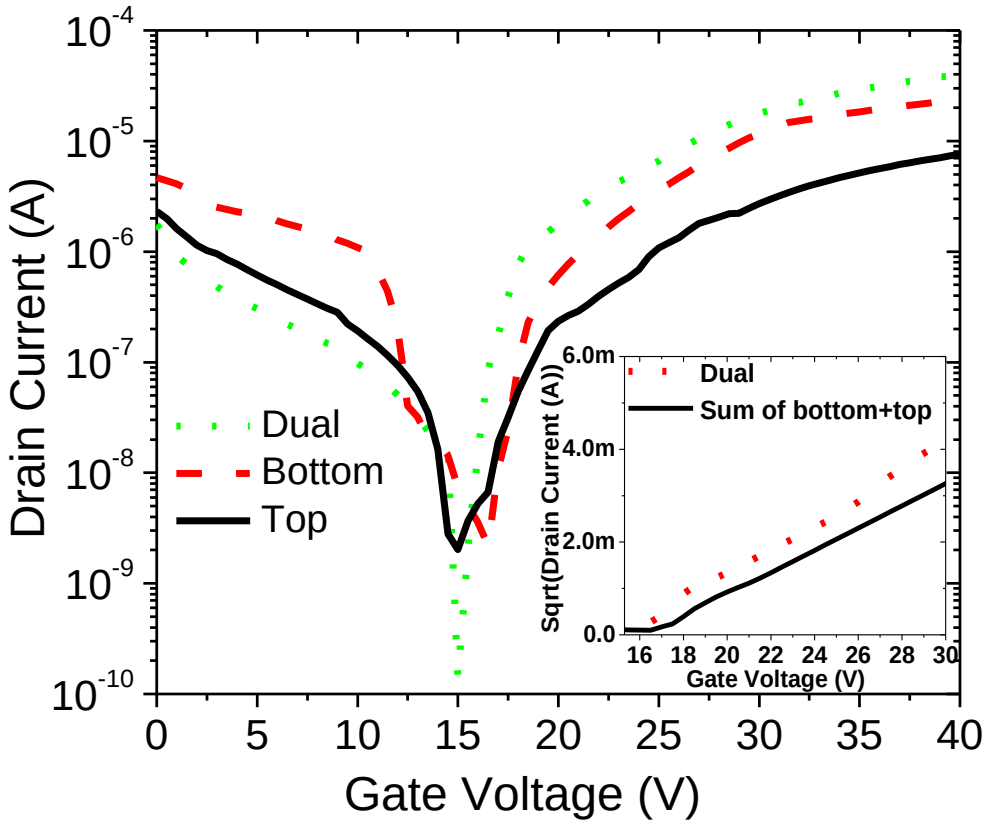


Figure 4.6 The transfer characteristics of ambipolar PDPP-TBT TFTs in top, bottom and dual gate mode: The inset shows that the current density from a dual-gate is larger than the sum of both the top- and the bottom- gate mode operation. Copyright 2012. IEEE

In order to further investigate the characteristics of dual-gate devices, we measured the S.S. By using two different gate insulator materials, dual-gate structures combine two different devices with different interface characteristics in a single device. The S.S. is a key figure of merit to characterize interfacial quality. In the case of a top-gate structure, D139 is employed as the gate dielectric whereas in the case of a bottom - gate structure silicon dioxide is the gate insulator. As shown in Figure 4.7, two different slopes in the sub-threshold region are observed. Two different slopes in the direction from off-state to on-state mean that two channels in dual-gate structure are formed and influenced by different interface characteristics sequentially.

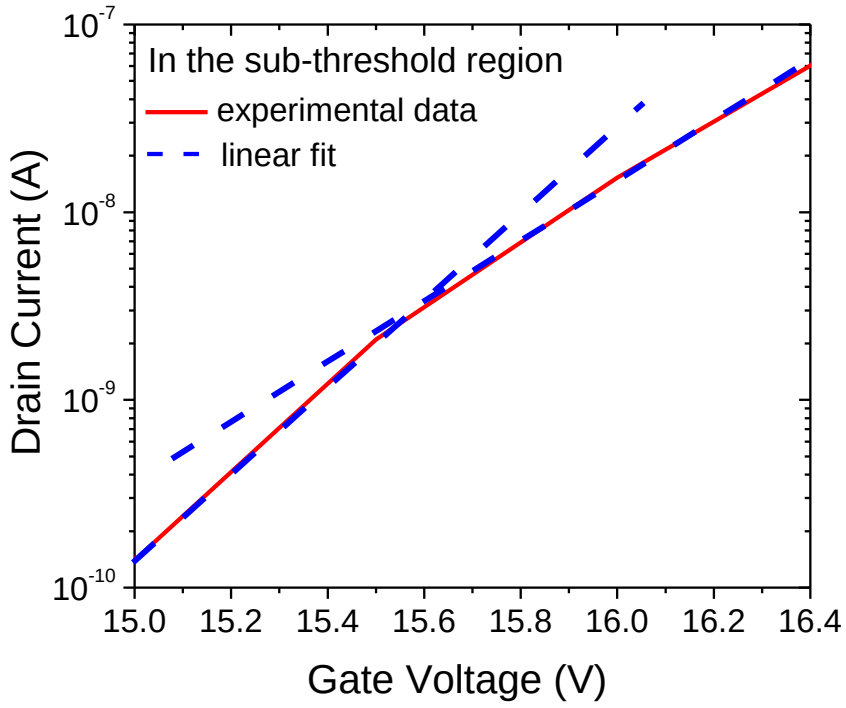


Figure 4.7 The sub-threshold slope in dual-gate mode operation of PDPP-TBT TFTs. Copyright 2012. IEEE

4.4 Charge carrier velocity distributions in ambipolar polymer FETs

4.4.1 EXPERIMENTS

Figure 4.8 shows that the transient response as a function of drain resistance value. It is seen that when the drain resistance is less than 5 kohm, the dynamic response is no longer a function of drain resistance. The 5 kohm resistor represents the limiting value of drain resistance at which the overall dynamic response is not determined by the RC time constant of the measurement circuit (comprising the drain resistance and the input capacitance of the oscilloscope as well as parasitics). Under these conditions, the distribution in arrival times of charge carriers at the drain electrode can be determined by an analysis of the response.

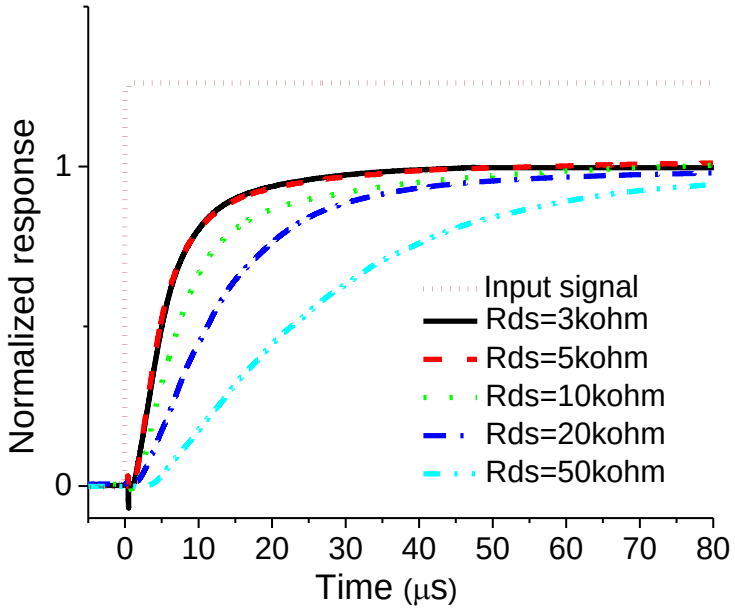


Figure 4.8 The normalized transient response of ambipolar PDPP-TBT TFTs as a function of Rds. Copyright 2012. IEEE

4.4.2 Results

Figure 4.9 shows the normalized transient response and velocity distribution of PDPP-TBT FETs in electron-enhancement as well as hole-enhancement modes. These samples had been exposed to air for some time and as a result, the mobilities are lower than those measured in pristine devices. The drop in electron mobility is greater than the drop in hole mobility. In the electron-enhancement mode, the time to reach quasi-equilibrium is much longer, which indicates that carriers arrive more "slowly". Slow arrival of electrons indicates greater degree of trap mediated charge transport as compared to hole transport. The independent determination of the velocity distributions for electrons and holes is a useful characterization method that can yield a lot of information about the materials being investigated.

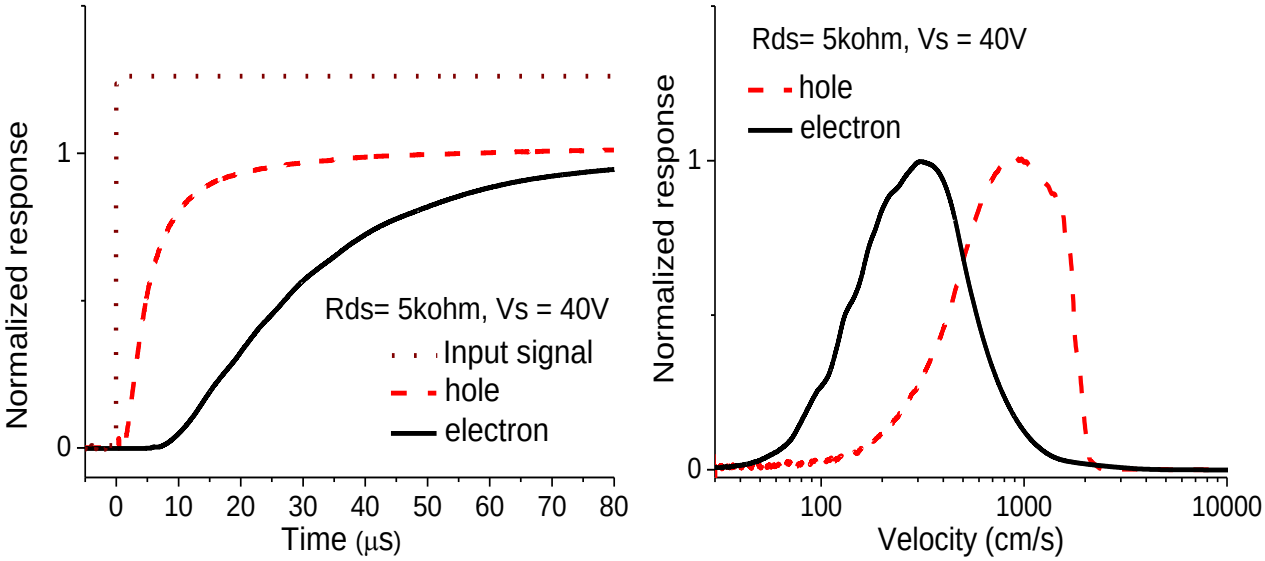


Figure 4.9 a) the normalized transient response and b) velocity distribution of ambipolar PDPP-TBT TFTs in electron- and hole-enhancement modes. Copyright 2012. IEEE

4.5 Charge transport and density of trap states in balanced high mobility ambipolar organic TFTs

4.5.1 Experiments

Temperature-dependent field-effect mobility measurements were performed from 120 K to 300 K with bottom-gate bottom-contact PDPP-TBT TFTs. There was a stability problem at low temperatures in the top-gate configuration. For this reason, temperature dependent measurements are reported only for bottom gate devices. The device characteristics of bottom-gate bottom-contact PDPP-TBT TFTs were re-measured at room temperature after temperature cycling and were almost unchanged compared to initial characteristics. The contact resistance is not expected to be dominant in these experiments due to the long channel length and a SAM treatment.

4.5.2 Results

Figure 4.10 (a) and (b) show the plot of field-effect mobility vs. reciprocal temperature in both hole- and electron-enhancement modes with applied gate voltages (depending on polarity). The field-effect mobilities of both electrons and holes decrease with temperature, as it expected for thermally activated transport [32, 131]. Figure 4.10 (c) and (d) show the activation energy as a function of V_{GS}-V_{ON} for holes and electrons. V_{ON} is the turn-on voltage of the device at which significant carrier accumulation is observed. To determine V_{ON}, we first calculate dI_D/dV_G. The gate voltage at which it becomes positive is V_{ON}. The activation energy decreases with increasing V_{GS}-V_{ON} for

both holes and electrons. This decrease in activation energy fits the MTR model of charge transport [32, 131]. As the applied gate voltage increases, the Fermi level moves toward the band-edge, decreasing the measured activation energy. This behavior has been observed in several high mobilities organic field-effect transistors with active semiconductor layers such as pentacene or liquid crystalline polymers [132-133]. The rate at which the activation energy falls in dependent on the trap DOS. The value of μo is about 5 $cm^2/V\text{-}s$. The combination of a fairly high mobility and the activation energy of ~ 100 meV strongly suggest the charge transport is by multiple trap and release. The data appear to be consistent with the MTR model. The Vissenberg-Matters VRH model is suitable for lower mobility doped systems.

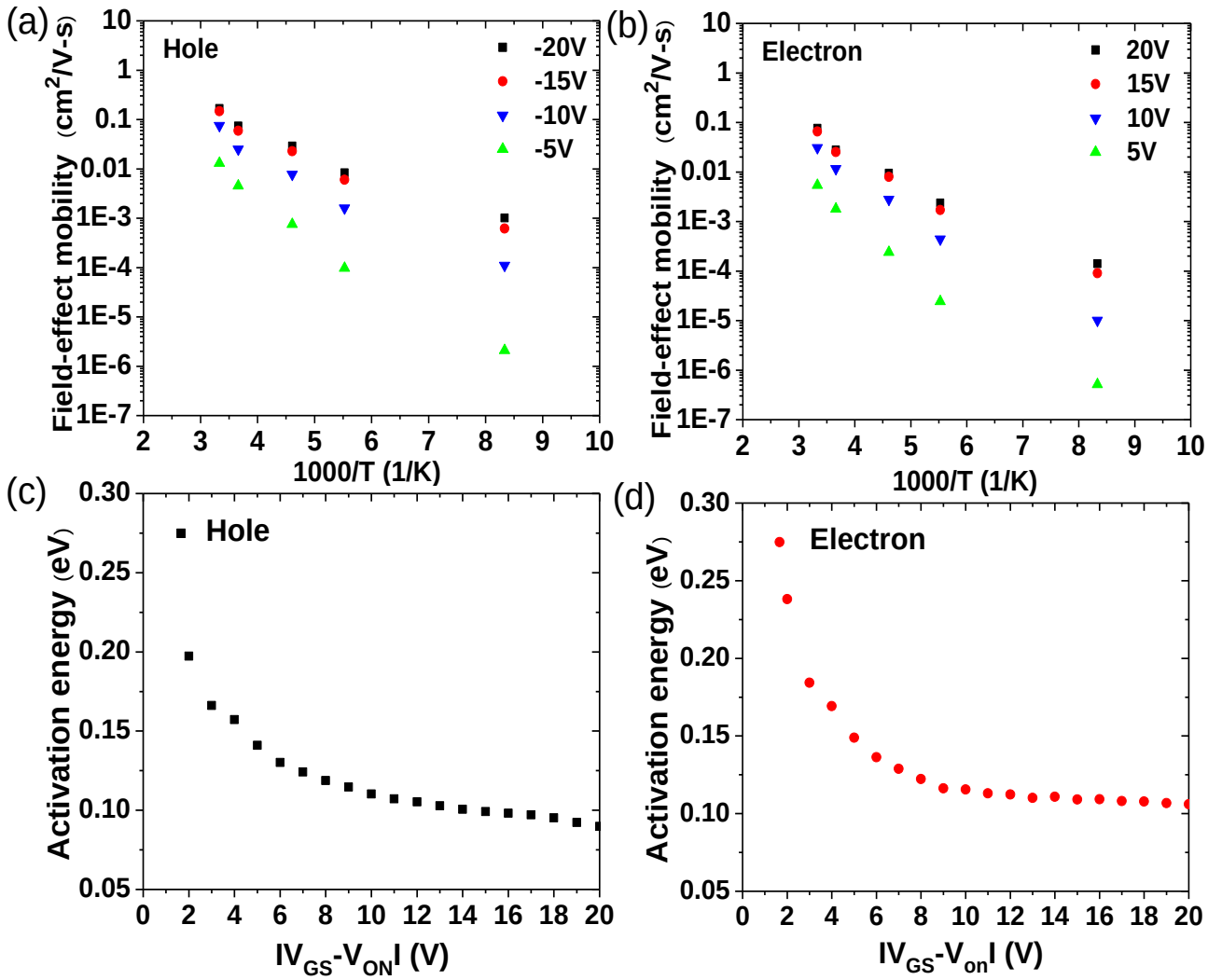


Figure 4.10 The plots of field-effect mobility vs. reciprocal temperature in both a) hole- and b) electron-enhancement modes in PDPP-TBT TFTs with V_{GS}-V_{ON} ranging from ±5V to ±20V and the activation energy as a function of V_{GS}-V_{ON} in c) holes and d) electrons. Copyright 2012. Elsevier

Figure 4.11 shows the density of trap states in the band gap of PDPP-TBT TFTs as calculated with two different methods as following.

$$N(E) = \frac{C_i}{qA}\left[\frac{\partial E_A}{\partial V_G}\right]^{-1} \quad (1)$$

$$N(E) = \frac{\partial}{\partial E_A}\left[\frac{\varepsilon_0 \varepsilon_i^2}{\varepsilon_s L} V_G \left(\frac{\partial E_A}{\partial V_G}\right)^{-1}\right] \quad (2)$$

where C_i is capacitance of gate dielectric, A is gate-voltage-independent effective accumulation-layer thickness, V_G is applied gate voltage and L is the thickness of gate dielectric. Equation 1 and 2 are derived by Lang *et al.*, and Kalb and Batlogg, respectively [104, 110]. Using C-V measurements, a value of 2.4 for the relative dielectric constant is obtained. The trap DOS depends critically on the rate of charge of activation energy with gate voltage. In particular, at high gate biases, the values of the trap DOS calculated by Equation 2 are quite different from those by Equation 1. This is a difference of two orders of magnitude between two methods, in which Equation 2 is more sensitive to variations in activation energy in the high gate bias regime. Similar observations have been also reported by Kalb and Batlogg [104].

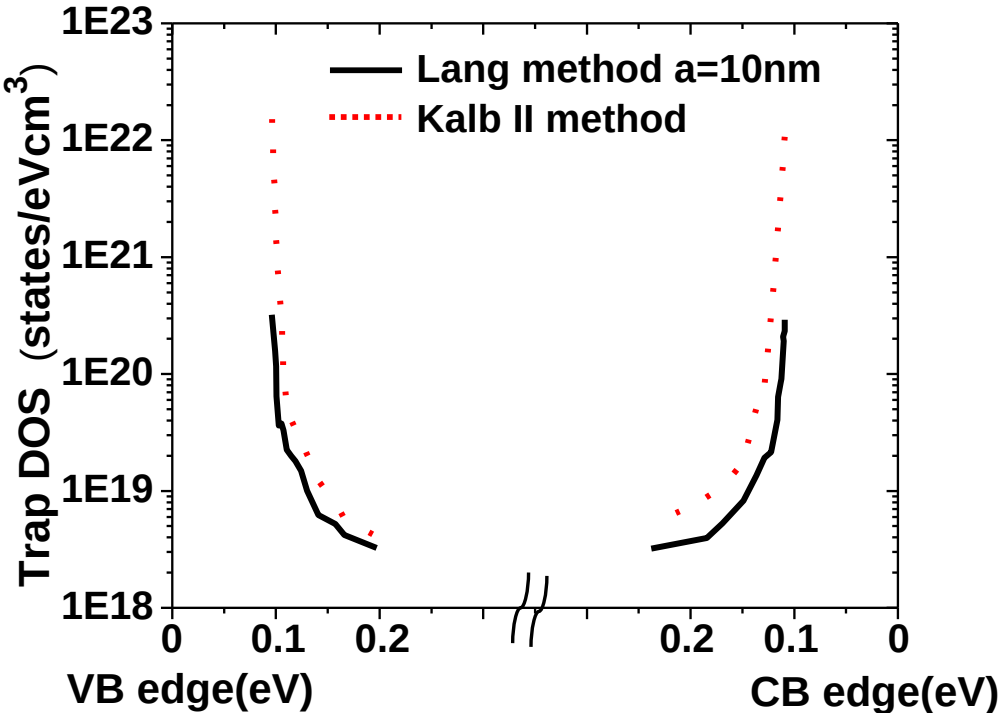
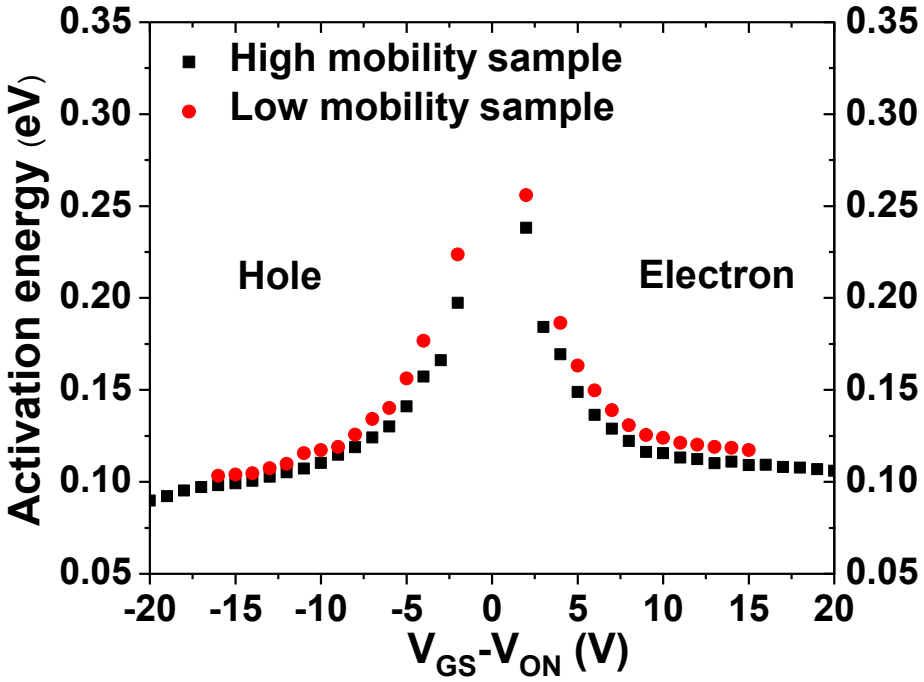


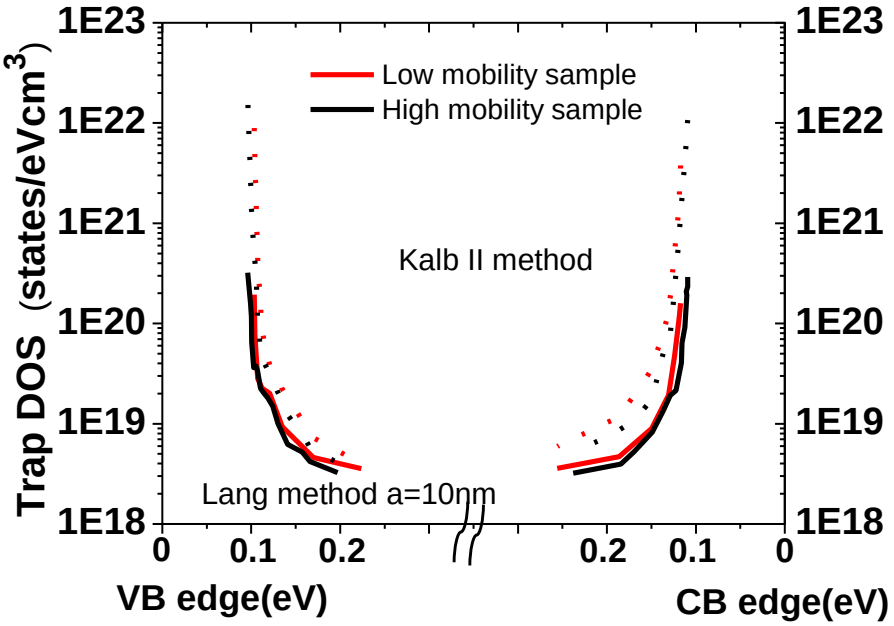
Figure 4.11 The density of trap states in the band gap as calculated with two different methods of Lang et al., and Kalb and Batlogg in PDPP-TBT TFTs. Copyright 2012. Elsevier

Experiments were performed with different device sets of bottom-gate bottom-contact PDPP-TBT TFTs to evaluate the effects of run-to-run variation. In a lower mobility set of samples compared to that reported above, the field-effect mobility is 0.13 $cm^2/V\text{-}s$ in hole-enhancement mode and 0.07 $cm^2/V\text{-}s$ in electron-enhancement mode. Figure 4.12 (a) shows the comparison of activation energy as a function of V_{GS}-V_{ON} between the high mobility sample and the low mobility sample for both holes and electrons. The low mobility sample possesses higher activation energy over the high mobility sample. The difference between high and low mobility samples is less than a

factor of two. Hence, the difference of the activation energy is not large. It is expected that the lower mobility PDPP-TBT TFTs possess a different density-of-trap states distribution. This is consistent with increased activation energy related with density of localized states. As shown in figure 4.12 (a), the increase in activation energy for the electrons is more than that of the holes. It is very likely that these variations in mobility are due to different degrees of exposure to air which affects electron transport more than hole transport [113, 134]. Upon long exposure to air, the electron mobility falls. This is fairly a common observation in n-channel FETs. The μo values of low mobility samples are also more than 4 cm^2/V-s at most temperatures. As shown in Figure 4.12 (b), the calculated trap DOS in the high mobility sample is less than that in the low mobility sample for a given energy, which is expected. This is confirmed by the trap DOS of holes and electrons calculated by Equation 2 which well reflects the difference of activation energy between the high and low mobility samples as compared to Equation 1.


High mobility sample
Low mobility sample
Hole
Electron
Activation energy (eV)
V_{GS}-V_{ON} (V)
0.35
0.30
0.25
0.20
0.15
0.10
0.05
-20
-15
-10
-5
0
5
10
15
20

(a)


Low mobility sample
High mobility sample
Kalb II method
Lang method a=10nm
Trap DOS (states/eVcm^3)
VB edge(eV)
CB edge(eV)
1E23
1E22
1E21
1E20
1E19
1E18
0
0.1
0.2

(b)

Figure 4.12 a) The comparison of activation energy as a function of VGS-VON and (b) the density of trap states in the band gap as calculated with two different methods of Lang et al., and Kalb and Batlogg in PDPP-TBT TFTs between high mobility sample and low mobility sample in both holes and electrons. Copyright 2012. Elsevier

The symmetry between the electron and hole transport characteristics, parameters and activation energies is remarkable. This is evident in the figures. We believe that our work is the first charge transport study of an ambipolar organic/polymer based field-effect transistor with room temperature mobility higher than 0.1 cm^2/V-s in both electrons and holes [135-136]. Polymers that have exhibited ambipolar behavior through the use of suitable dielectrics have hitherto generally exhibited low mobilities [137].

4.6 Conclusions

We have fabricated ambipolar organic FETs based on PDPP-TBT. The devices possess balanced electron and hole mobilities. These mobilities which are both > 0.5 cm^2/V-s are the highest observed in any ambipolar semiconductor with balanced mobilities at the time of their publication. The use of surface treatments with OTS-8 and PFBT and thermal annealing lowered electrical contact and reduced leakage current. In addition, we reported the characteristics of dual-gate FETs with two different gate dielectrics in a single device. Our results showed a reduction in the overall Vth as well as the non-saturating minority carrier current and the increase in on-current and the improvement in S.S. and on-off current ratio compared to single gate devices. We have

also studied velocity distributions of charge carriers under non-quasi-static conditions. Such measurements are helpful in understanding charge transport.

We have investigated charge transport studies on high mobility and balanced transport ambipolar PDPP-TBT TFTs. Through temperature and gate-bias dependent field-effect mobility measurements, the activation energies and trap DOS were calculated for electron and hole charge carriers. The decrease in activation energy with increasing V_{GS}-V_{ON} in both holes and electrons indicate that the main charge tranport mechanism in this orgnaic semiconductor is multiple trap and thermal release. The trap density of states in ambipolar PDPP-TBT TFTs has also been calculated using two analytical methods developed by Lang et al. and Kalb and Batlogg. The trap DOS depends on sample processing conditions, device geometry and history of the samples exposure to ambient conditions. This materials is unique in that there is appears to be delocalization of both holes and electrons as well as relatively low and symmetric trap distributions for both electrons and holes. This leads to the observed high electron and hole mobilities.

CHAPTER 5 CHARGE TRANSPORT IN POLYMER THIN-FILM TRANSISTORS BASED ON DIKETOPYRROLOPYRROLE-THIOPHENE COPOLYMER

5.1 Introduction

There have been very few polymer semiconductors reported to date with mobilities in excess of 1 cm^2/V-s. One of promising approaches to realize high mobility polymers is to design copolymers reinforcing intramolecular interactions, which results in enhanced molecular π-orbital overlap and facile intermolecular charge transport [138-141]. One such family of copolymers is based on the donor-acceptor architecture and utilizes the diketopyrrolopyrrole (DPP) acceptor block. Recently, good performance in solution-processable OFETs based on DPP has been reported with mobilities of 2-8 cm^2/V-s [142]. We expect that due to the donor-acceptor interaction, DPP-based materials will exhibit different transport characteristics from those reported for thiophene-based polymers [143-144]. Studies of charge transport can provide important information in better understanding the origins of high mobility in some of DPP-based systems. We also note that quasi-DC experiments provide only a partial picture charge transport and device physics in high mobility DPP based FETs. For this reason, we perform non-quasi-static (NQS) measurements which enable time-resolved charge transport studies including the computation of carrier velocity distributions at different measurement temperatures. [97-99].

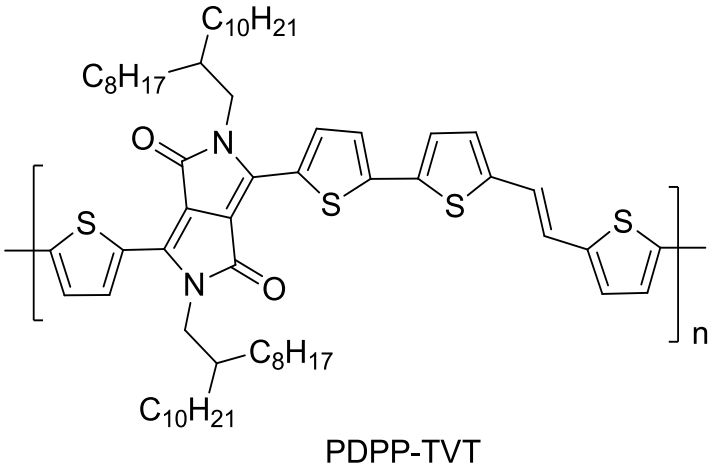
In this chapter, we report on the device physics and charge transport characteristics of high-mobility dual-gate FETs with active semiconductor layers

consisting of PDPP-TVT. This polymer is one of the most promising among DPP-based polymers, which have recently been shown to possess high field-effect mobility [142-143]. Steady-state and NQS measurements have been performed to extract key transport parameters and velocity distributions of charge carriers in this copolymer. It must also be noted that we employed a 4-point-probe configuration to measure field-effect mobility in the linear region to enable more accurate mobility and activation energy measurements, especially at low temperatures. We also compare the activation energy vs. field-effect mobility in a few important polymer semiconductors to gain a better understanding of transport of DPP-systems and make appropriate comparisons. We also investigate the effect of solvents and post-annealing temperatures on PDPP-TVT semiconductors based TFTs.

5.2 Diketopyrrolopyrrole-thiophene copolymer

A brief description of the synthesis of this polymer is provided after the more detailed description published by Dr. Prashant Sonar *et al*., who provided the material for this study [143]. To a Schlenk flask, (E)-1,2-bis(5-trimethylstannyl)thiophen-2-yl-ethene (0.176 g, 0.34 mmol), 3,6-bis-(5-bromo-thiophen-2-yl)-N,N'-bis(2-octyldodecyl)-1,4-dioxo-pyrrolo[3,4-c]pyrrole(0.350g,0.34mmol)and (bis(triphenylphosphine)palladium(II) dichloride (20 mg, 0.02 mmol) were added under vaccum for 25 min and then argon-vaccum cycles were repeated three to four times. The anhydrous toluene (15 mL) purged under arogn was then added to the above compounds and the solution was stirred under argon for 30 min. The reaction mixture was raised to 90^{o}C and stirred for 48 hours.

Bromobenzene (0.5 mL) was added to the reaction mixture to react further with the residual trimethylstannyl end group and the mixture was further stirred at 90 °C for 4 h. The mixture was cooled down to room temperature and then poured into stirring methanol (200 mL), filtered off, washed with methanol, and dried. The solid was then further purified by Soxhlet extraction using acetone (24 h), hexane (24 h), and then dissolved with chloroform. Yield: 0.250g (72%). GPC (HT-GPC measurements at 160 ^{o}C; 1,2,4-trichlorobenzene as eluent; polystyrene as standards). Mw/Mn (GPC)= 10,580/ 25,680, polydispersity index (PDI) =2.42.



PDPP-TVT

Figure 5.1 Synthesis of PDPP-TVT

5.3 Characteristics of high mobility polymer FETs based on diketopyrrolopyrrole-thiophene Copolymer

5.3.1 EXPERIMENTS

Device fabrication started with an n-type silicon substrate with a resistivity of 1-10 Ωcm. This substrate was also used as the bottom-gate electrode. This silicon substrate was thermally oxidized resulting in a 200 nm thick silicon dioxide films, which functions as the bottom-gate insulator. A 52.5 nm thick titanium /gold (2.5 nm/50 nm) bi-layer was deposited by thermal evaporation for source and drain electrodes. These samples were immersed in a dilute octadecyltrimethoxysilane (OTMS) solution with isopropanol (concentration= 1:20) for 5 minutes under the nitrogen atmosphere [145]. The substrate was rinsed with isopropanol, and dried under a nitrogen flow. The substrates were placed on the hot plate at 120 °C for 30 minutes. The PDPP-TVT solution was formed using chloroform as the solvent (8 mg/mL concentration). A 40 nm thick semiconductor film was formed by spin-coating and then pre-annealed at 200 ºC for 30 minutes. Next, a polymeric D139 (supplied by MERCK) dielectric as a top-gate insulator was deposited of which capacitance value is ~ 4 nF/cm^2. Finally, a 50 nm thick patterned gold as a top-gate electrode was deposited by thermal evaporation. The devices possess a channel width of 1000 μm and a channel length of 50 μm. In order to mitigate the effect of contact resistance, a 4-point-probe measurement was employed for investigating linear region operation. The source/drain electrodes were defined by photolithography and titanium/gold (2.5 nm/50 nm) bi-layers were deposited by thermal evaporation. The dimension of devices is a channel width of 1000 μm, a channel length of 20 μm and effective channel length of 8 μm.

5.3.2 RESULTS

Figure 5.2 and 5.3 show the output and the transfer characteristics and field-effect mobility of a top-gate and bottom-gate TFTs based on PDPP-TVT operating in linear and saturation regions. The output and the transfer characteristics show good electrical performance with on-off current ratio as high as 10^6-10^8 *in air*. In top-gate operation, the output characteristics exhibit lower electrical contact resistance compared to bottom-gate operation. This is because the injection area of top-gate bottom-contact operation (~μm^2) is much larger than bottom-gate bottom-contact operation (~nm^2). Top-gate PDPP-TVT TFTs possess the up to 1.3 cm^2/V-s in the linear region and 2.6 cm^2/V-s in the saturation region, as shown in Figure 5.2, and bottom-gate PDPP-TVT TFTs possess the up to 0.8 cm^2/V-s in the linear region and 1.1 cm^2/V-s in the saturation region, as shown in Figure 5.3.

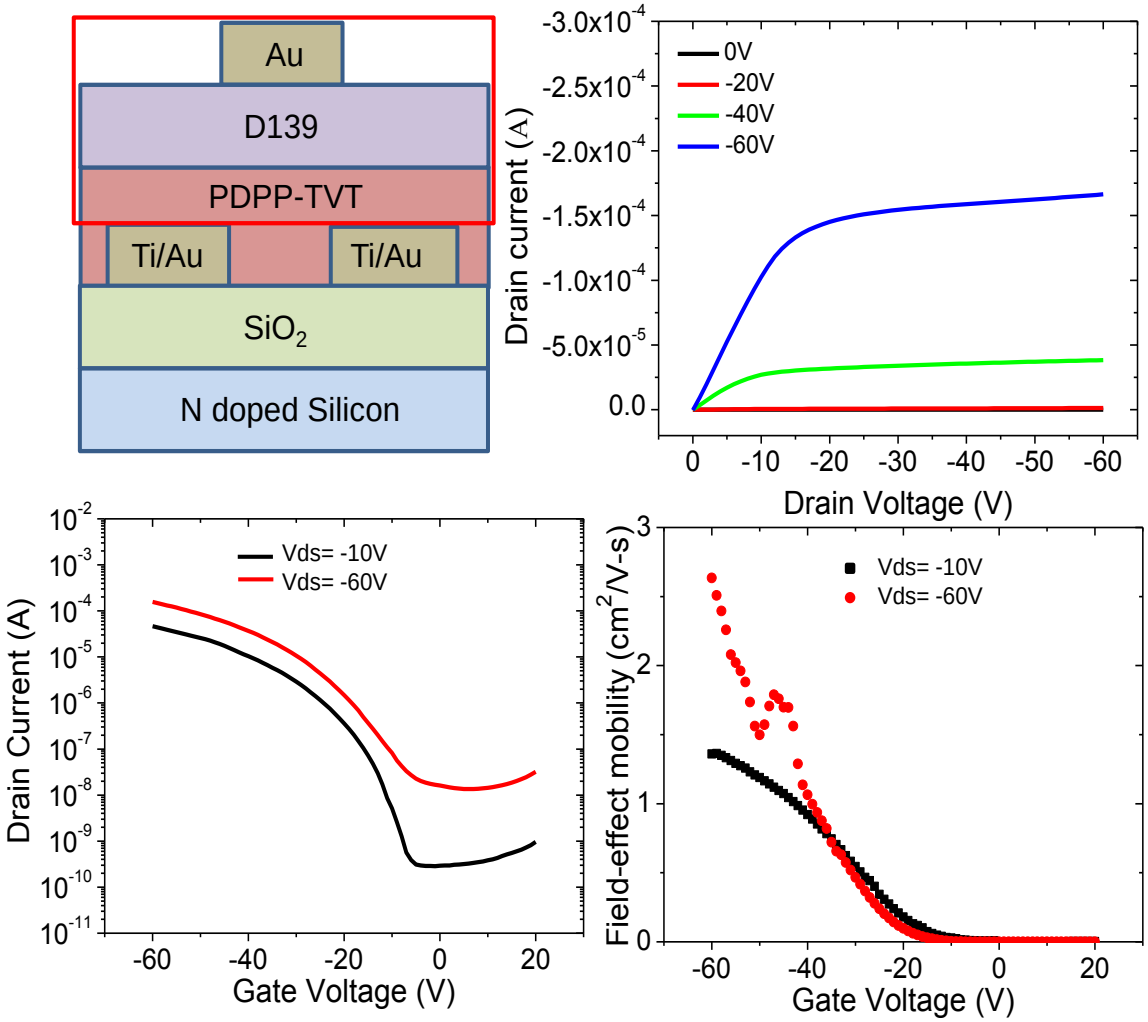


Figure 5.2 (a) The schematic cross section (b) the output characteristics, (c) the transfer characteristics and (d) the field-effect mobility vs. gate bias of top-gate PDPP-TBT TFT operating in linear and saturation regions

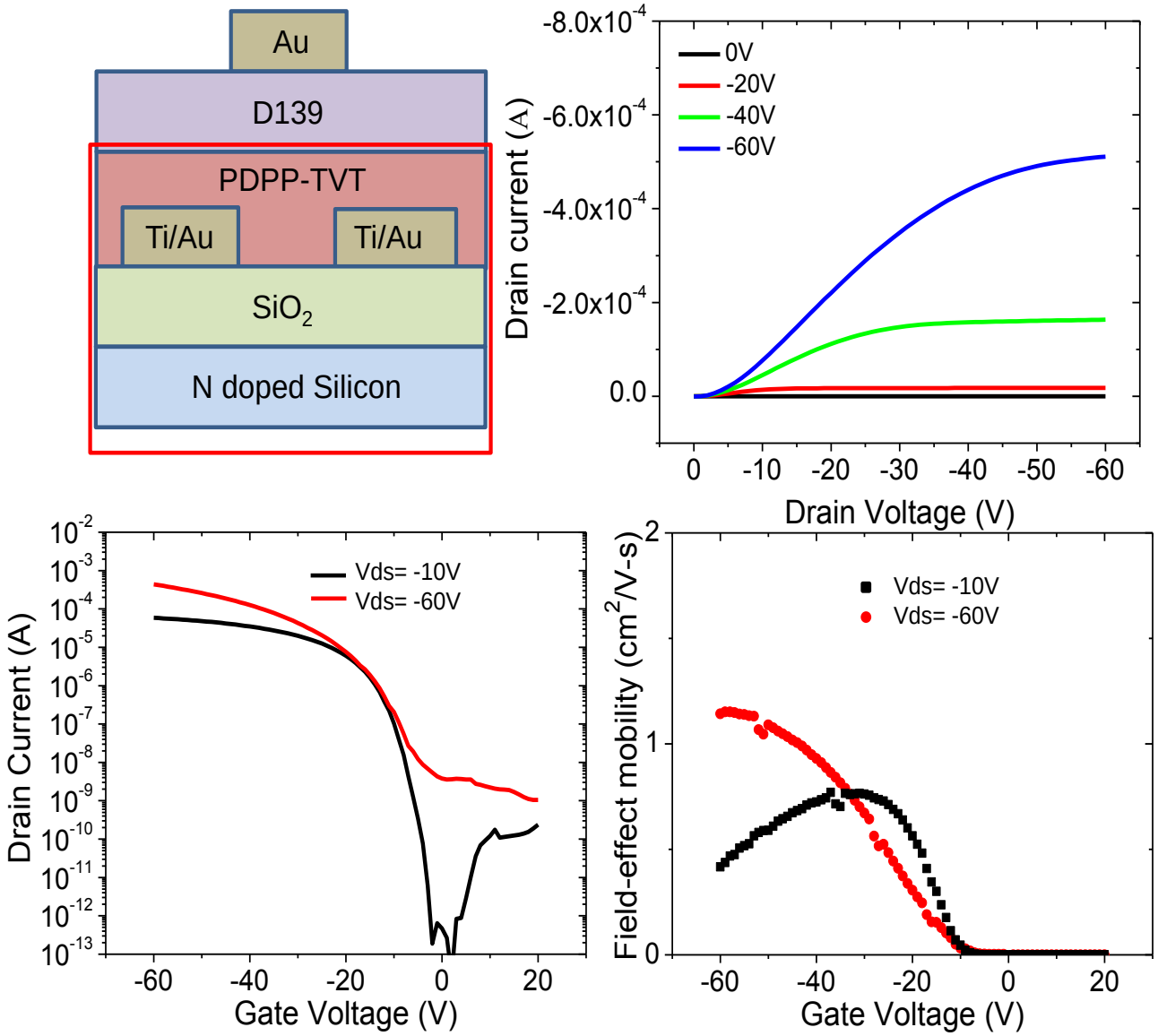
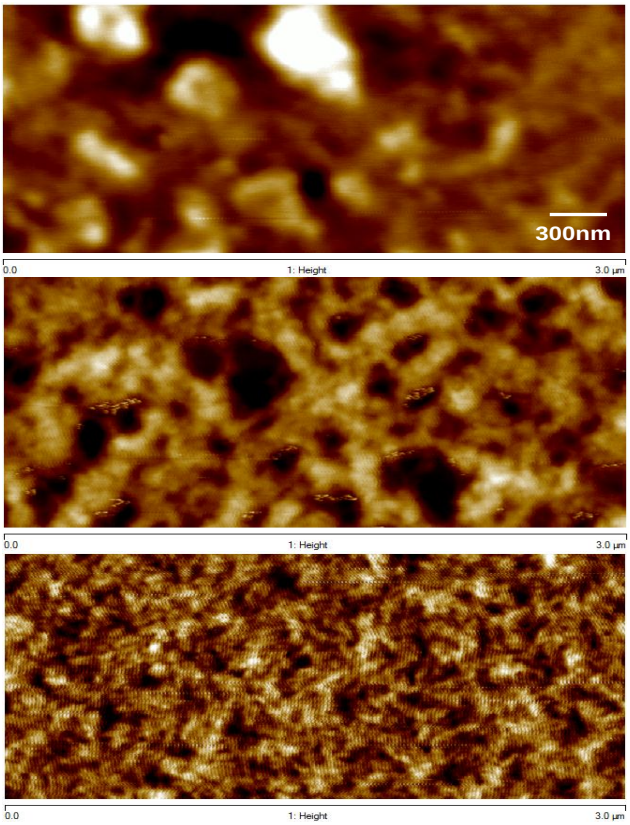
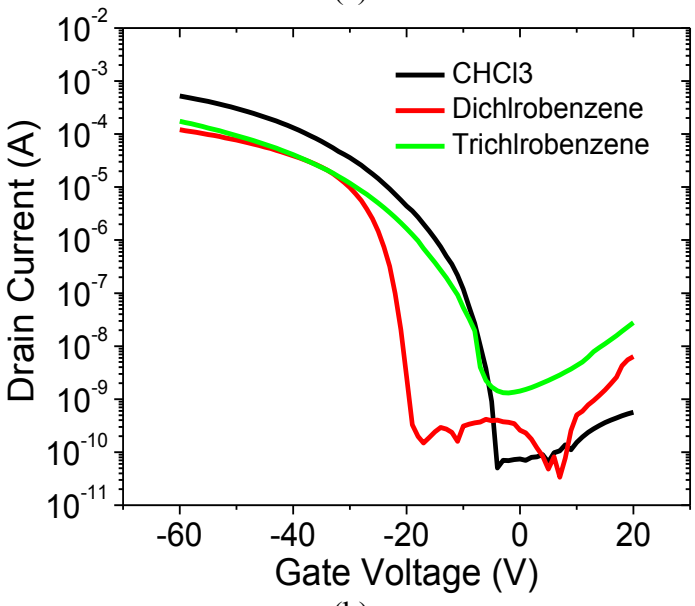


Figure 5.3 (a) The schematic cross section (b) the output characteristics, (c) the transfer characteristics and (d) the field-effect mobility vs. gate bias of bottom-gate PDPP-TBT TFT operating in linear and saturation regions

Figure 5.4 (a) shows the AFM images of PDPP-TVT films deposited with different solvents. The film formed with chloroform exhibits larger grain size with more condensed and connected domain-morphology compared to the films formed with dichlorobenzene or trichlorobenzene. Well-organized or -connected bigger grains result in better charge transport, which indicates better device performance in FETs [109]. This is supported by the transfer characteristics in PDPP-TVT FETs with different solvents, as shown in Figure 5.4. The field-effect mobility in the linear region with chloroform is 1.3 cm^2/V-s whereas those with dichlorobenzene and trichlorobenzene are 0.5 and 0.6 cm^2/V-s, respectively. Compared to dichlorobenzene or trichlorobenzene, the use of chloroform increases the field-effect mobility by more than a factor of two as well as decreases the off-current and S.S.



(a)



(b)

Figure 5.4 AFM images of PDPP-TVT films with chloroform, dichlorobenzene and trichlorobenzene (from the top to bottom) and (b) transfer characteristics of PDPP-TVT FETs with different

As discussed above, post-deposition thermal annealing improves the crystallinity or molecular ordering of the polymer thin films [107-108]. Figure 5.5 shows the AFM images of PDPP-TVT films and the transfer characteristics and extracted field-effect mobilities in PDPP-TVT FETs with different post-annealing temperatures. For the sample annealed at 200 ºC, the polymer packing is improved compared to at room temperature and 140 ºC. However, at the annealing temperature of 300 ºC, the polymer film is damaged.

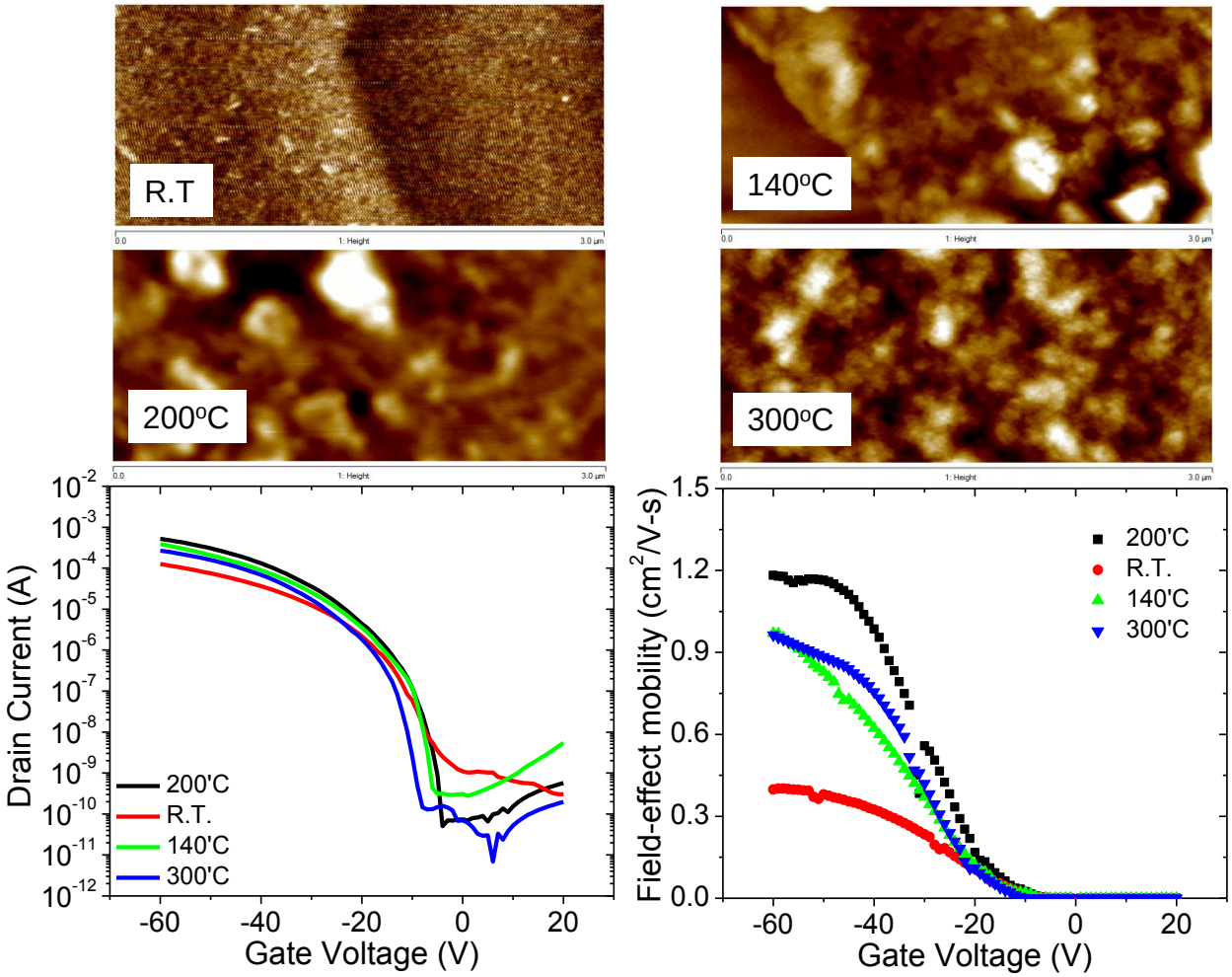


Figure 5.5 the AFM images of PDPP-TVT film and the transfer characteristics and extracted field-effect mobilities in PDPP-TVT FETs with different post-annealing temperatures

Solid state ordering and molecular packing of the polymeric chains governs the charge carrier transport across the intra and intermolecular network of the bulk polymer. X-ray diffraction (XRD) analysis was carried out in order to study the packing behavior and orientation effect of PDPP-TVT. For this study, we used several micron thick polymer flakes. These polymer flakes were prepared by removing the solvent from polymer solution (prepared in chloroform) followed by rinsing the thick layer of polymer deposited on the flask by using methanol (anti-solvent for polymer). The polymer flakes were cut into small piece for the 2D-XRD measurement. The 2D-XRD diffraction pattern and 2D-XRD image for the PDPP-TVT is shown in Figure 5.6 when the incidence X-ray is perpendicular to the flakes. Two peaks were observed in the diffractogram which are attributed to the interlayer d-spacing and π-π stacking respectively. The primary (100) strong peak at $2\theta = 4.76°$(θ is X-ray diffraction angle) corresponds to the reflection of the crystal plane with an interlayer d-spacing of 18.54 Å. A shorter interlayer spacing distance is due to the close inter-digitation of the alkyl side chains in adjacent layers. The peak located at $2\theta = 9.50°$ is associated with the second order diffraction peak of the primary (100) peak. Such a multiple peaks in the XRD diffractogram is a clear signature of the better ordering and high crystallinity of the polymeric material. The secondary peak (010) was measured at $2\theta = 24.95°$ and the distance calculated for this peak is around 3.56 Å which is assigned for π-π stacking. Such a shorter π-π stacking distance between polymer chains in the conjugated backbone indicates the high degree of intermolecular interactions arising from the fused aromatic donor (TVT) and acceptor (DPP) blocks present in the backbone. High degree of coplanarity, highly π-extended

conjugated backbone and strong D-A interactions are responsible parameters for the small π-π stacking value. These (interlayer d-spacing and π-π stacking) values are in a well agreement with the earlier reported high mobility DPP based polymeric semiconductors. The corresponding 2D-XRD image in inset also clearly exhibits the ordering pattern for primary (100) and (010) secondary diffraction peaks with strong visible diffraction rings.

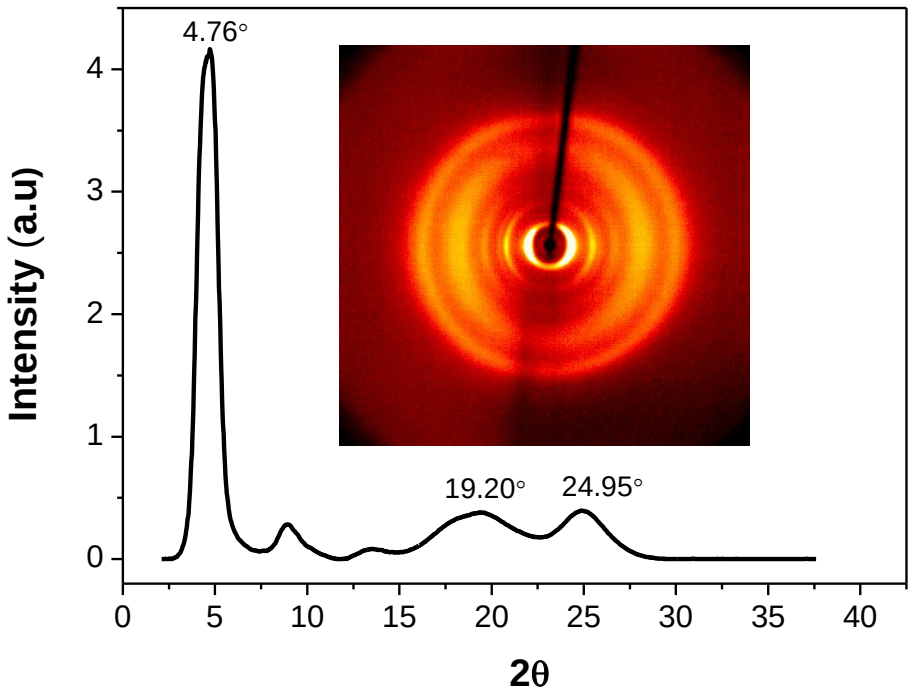


Figure 5.6 2D-XRD pattern intensity graphs (right) and 2D-XRD image (left) obtained with the incident X-ray perpendicular to the thin film stack of PDPP-TVT copolymer.

5.4 Charge transport measurements in steady-state and under non-quasi-static conditions in dual-gate PDPP-TVT FETs

5.4.1 EXPERIMENTS

Figure 5.7 shows the optical image of PDPP-TVT FET employing 4-point-probe configuration. For low electric field between source and drain electrodes ($|V_{DS}| < |V_G - V_T|$), the drain current I_D is given by

$$I_D = \frac{W\mu_{lin.}C_i}{L} \times \left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right)$$

where W, L, C_i, V_G, and V_T represent the channel width, the channel length, the capacitance of the gate dielectric per unit area, the gate voltage, and the threshold voltage, respectively. However, high electrical contact resistance leads to an underestimation in field-effect mobility extracted by the equation above, which will affect activation energy calculations and also velocity distributions. The 4-point-probe measurement can compensate for the non-ideal electrical contact between electrode and channel caused by an injection-barrier [146-147]. As shown in Figure 5.7, additional two probes are employed in the channel region. The distance and the voltage difference between those probes become the effective channel length and effective drain voltage, respectively. The corrected field-effect mobility can be extracted from following revised equation.

$$I_D = \frac{W\mu_{lin-eff.}C_i}{L_{eff}} \times \left((V_{GS} - V_T)V_{DS*} - \frac{V_{DS*}^2}{2} \right)$$

where $\mu_{lin\text{-}eff}$, L_{eff}, and V_{DS*} represent the effective linear mobility, effective channel length and the effective drain voltage, respectively.

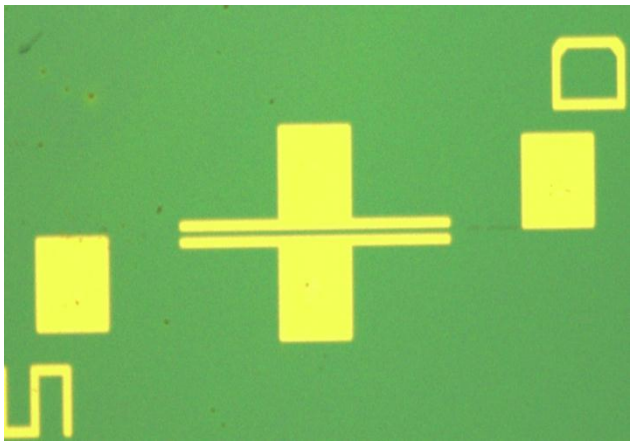


Figure 5.7 The optical image of PDPP-TVT FET employing 4-point-probe configuration.

Figure 5.8 shows that the transient response as a function of drain resistance value. It is seen that when the drain resistance is less than 3 kΩ, the dynamic response is no longer a function of drain resistance.

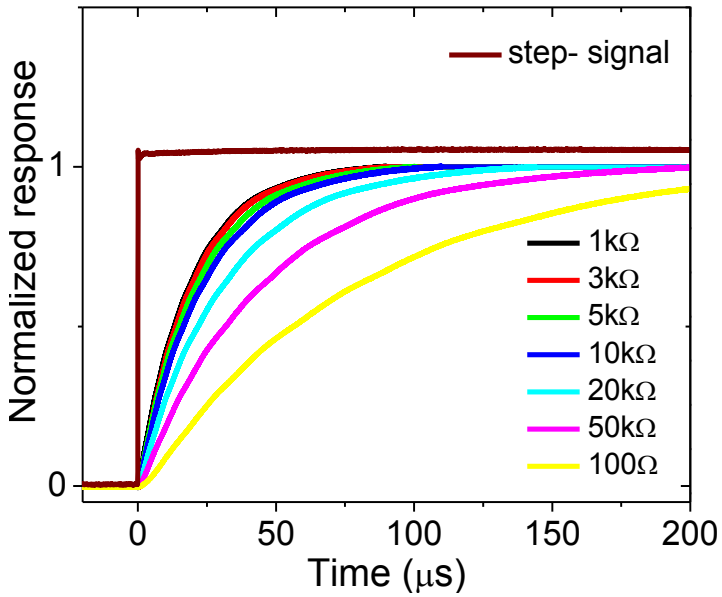


Figure 5.8 The normalized transient response of PDPP-TVT TFTs as a function of R_{ds}

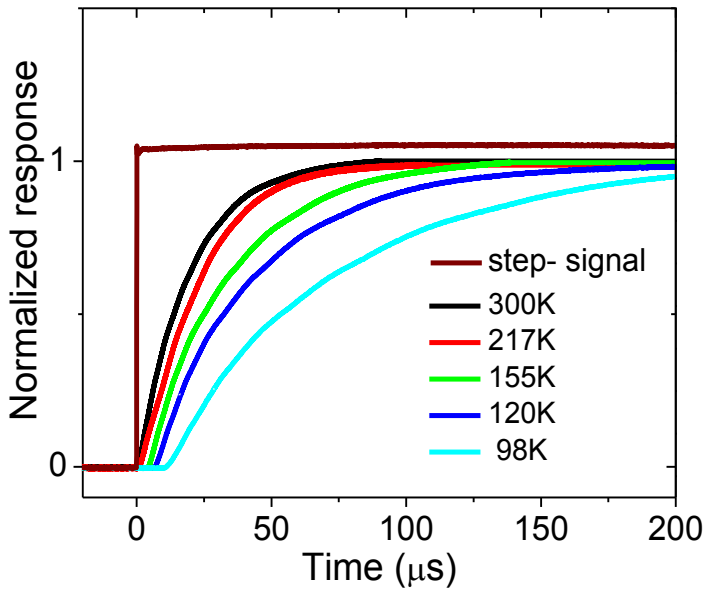
5.4.2 Results

Temperature-dependent velocity distribution measurements were performed from 98 K to 300 K on PDPP-TVT TFTs. The device characteristics of PDPP-TVT TFTs were re-measured at room temperature after temperature cycling and were largely unchanged compared to the initial characteristics. Figure 5.9 (a) shows that the "turn-on time" and the time to reach quasi-equilibrium beyond the "turn-on time" become longer with decreasing temperatures. Shift to lower velocities in corresponding velocity distributions observed in Figure 5.9 (b) supports such transport characteristics with decreasing temperatures. Complicated dynamic response characteristics such as bimodal distributions with two distinguishable peaks previously reported in diketopyrrolopyrrole-naphthalene copolymer FETs are not observed in PDPP-TVT FETs at low measurement temperatures. We believe that better homogeneity in charge carrier transport is obtained in the case of PDPP-TVT resulting in spatially uniform trap distributions and charge injection even at low measurement temperatures. Figure 5.9 (c) shows the comparison of field-effect mobility as a function of temperature between DC and dynamic measurements. The effective dynamic mobility can be extracted by following equation [97-98,148-150]

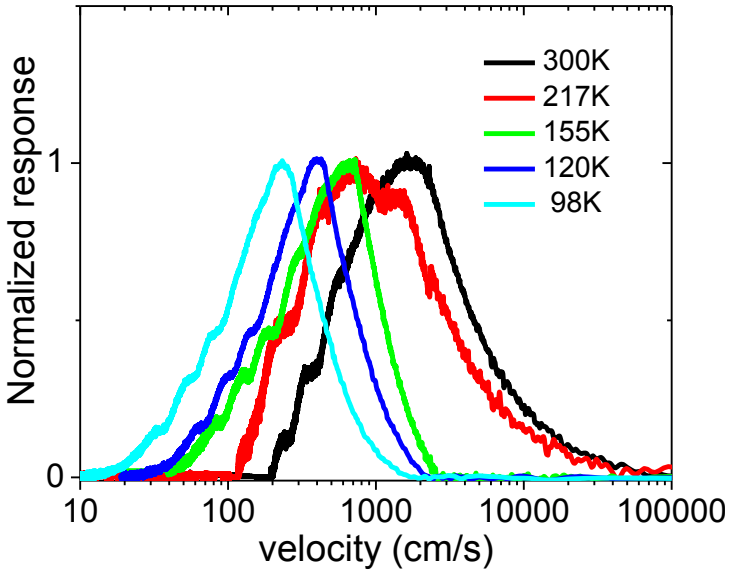
$$\mu_{dynamic} = 0.38 \frac{L^2}{\tau (V_{GS} - V_T)}$$

Where τ is "turn-on time". Thermally activated transport is observed in the case of such dynamic measurements with a similar activation energy value as DC measurement. Activation energy extracted by dynamic measurement is slightly larger than that

extracted by DC measurement. This suggests that carrier density effects are more important than bias stress in determining mobility. The mobility extracted from the dynamic measurement is at a lower average carrier density in the channel since quasi-equilibrium is not yet achieved during the measurement.



(a)



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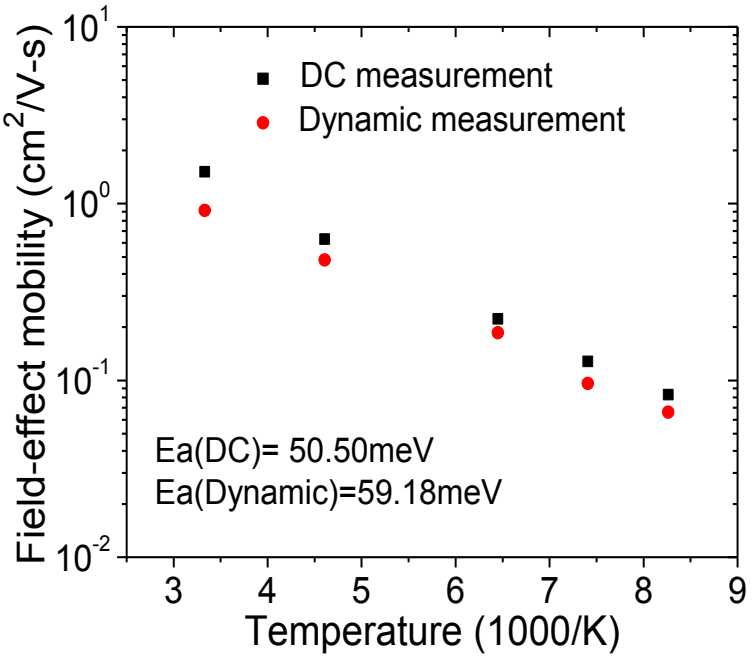


(c)

Figure 5.9 Temperature-dependent measurements from 98 K to 300 K on PDPP-TVT TFTs : (a) the normalized transient response (b) velocity distributions of charge carriers and (c) the comparison of field-effect mobility as a function of temperature between DC and dynamic measurements

Figure 5.10 shows the results obtained by temperature-dependent field-effect mobility measurements in dual-gate PDPP-TVT FETs. The plot of field-effect mobility vs. reciprocal temperature with applied gate voltages ranging from 0V to -60V demonstrates that the field-effect mobilities decreased with temperature and increased with applied gate voltage in both bottom- and top-gate operation.

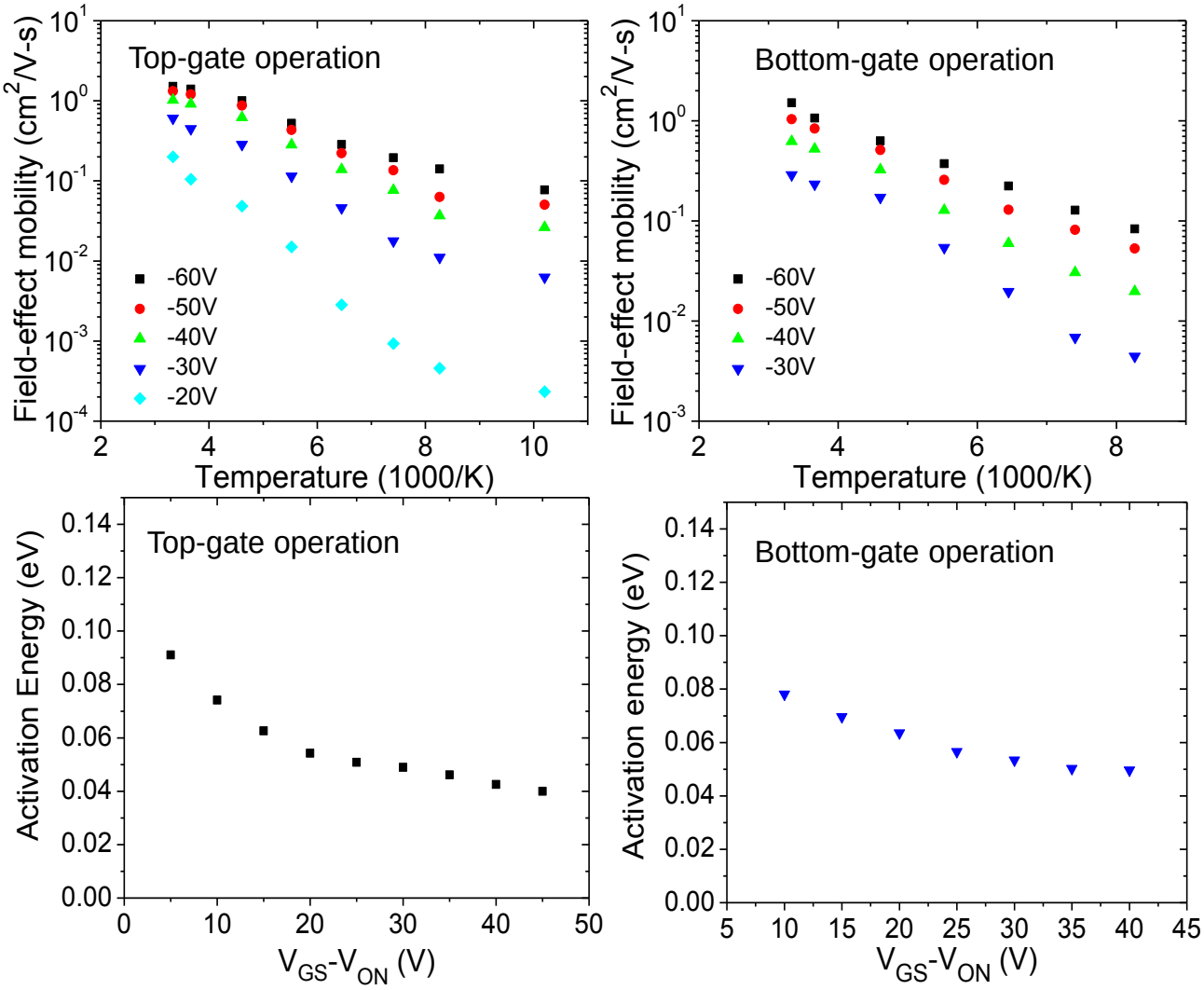


Figure 5.10 Temperature-dependent field-effect mobility measurements from 98 K to 300 K on dual-gate PDPP-TVT FETs

Figure 5.11 shows the plot of activation energy versus V_{GS}-V_{ON} in bottom- and top-gate operations. The activation energy decreases with increasing V_{GS}-V_{ON} in both bottom- and top-gate operations. This decrease in activation energy fits the MTR model or Monroe-type model of charge transport [31-33, 151]. Significantly, the plot extracted from 4-point-probe measurements exhibits a clear Arrhenius behavior, from which an

accurate activation energy, unaffected by contact resistance effects, can be extracted. We note that Chesterfield *et al.* observed that a series resistance between the gated channel and the electrodes affects activation energy [152]. Figure 5.12 shows the plot of the field-effect mobility as a function of $T^{-1/2}$ and $T^{-1/4}$ at the fixed carrier concentration of $2.7x10^{12}$ cm^{-2} [29-30]. The clear deviation from expected behavior for VRH shows that VRH theories are not particularly applicable for this material. Instead, the data indicate that an MTR or Monroe-type model of transport is more relevant. In the Monroe-type model, the activation energy corresponds to the energy difference between the Fermi level and a hypothetical transport level. The MTR model is essentially a Monroe-type model in which the transport level is a band edge. The activation energy measured under top-gate operation is less than that under bottom-gate operation. Since the activation energy roughly corresponds to the energy distance between occupied trap states and the transport level, the electronic density of states close to the top-gate insulator is different from that close to the bottom-gate insulator, due to different trapping characteristics.

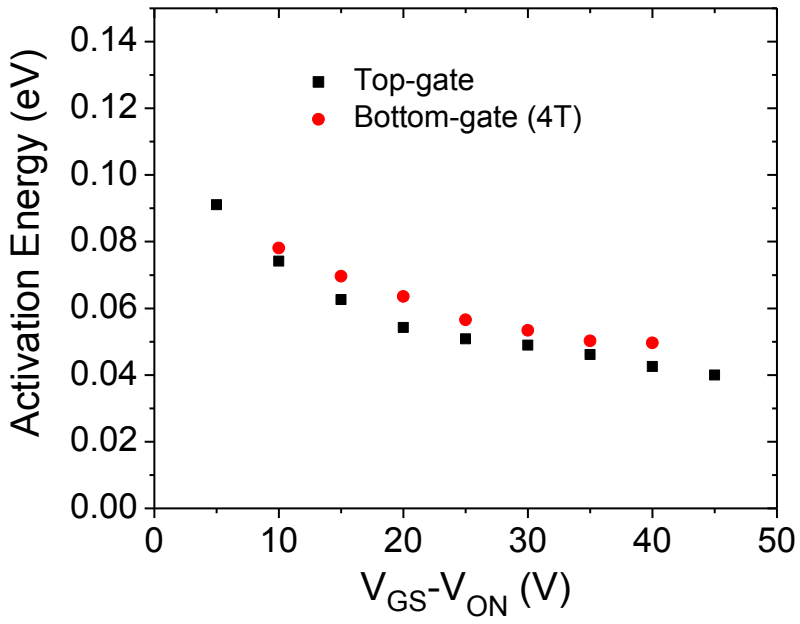


Figure 5.11 Activation energies with a function of VGS-VON in bottom- and top-gate operations

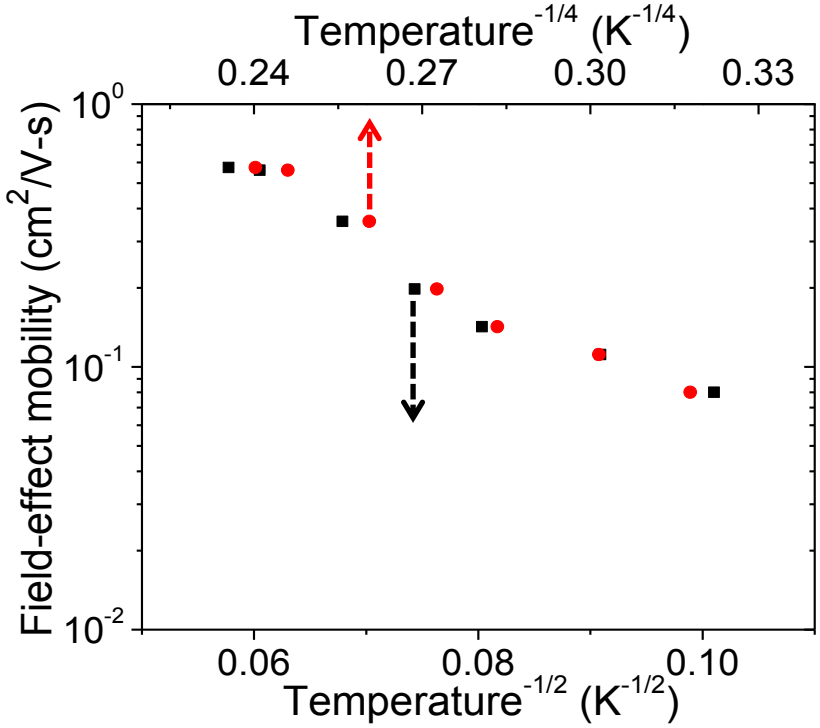


Figure 5.12 The plot of the field-effect mobility as a function of $T^{-1/2}$ and $T^{-1/4}$ at the fixed carrier concentration of $2.7x10^{12}$ cm^{-2} to check variable range hopping transport.

The magnitude of the lowest activation energy (~ 40 meV) is relatively small in comparison with measurements made with other DPP-based semiconductors. This is illustrated in Figure 5.13., which shows the activation energy as a function of carrier density measured in FETs made with three different DPP materials. There is a trend of decreasing activation energy with increasing mobility value for a given carrier density. Data in Figure 5. 13 suggest that even higher room temperatures – exceeding 10cm^2/V-s – are possible in these materials if the density of trap states is reduced so that the Fermi level can move into the π band at typical FET carrier densities. For such mobilities to be realized careful attention must be paid to molecular ordering and approached such as solvent vapor annealing or imprint assisted ordering that have proven to be successful with improving mobility other polymer/organic semiconductors might be useful.

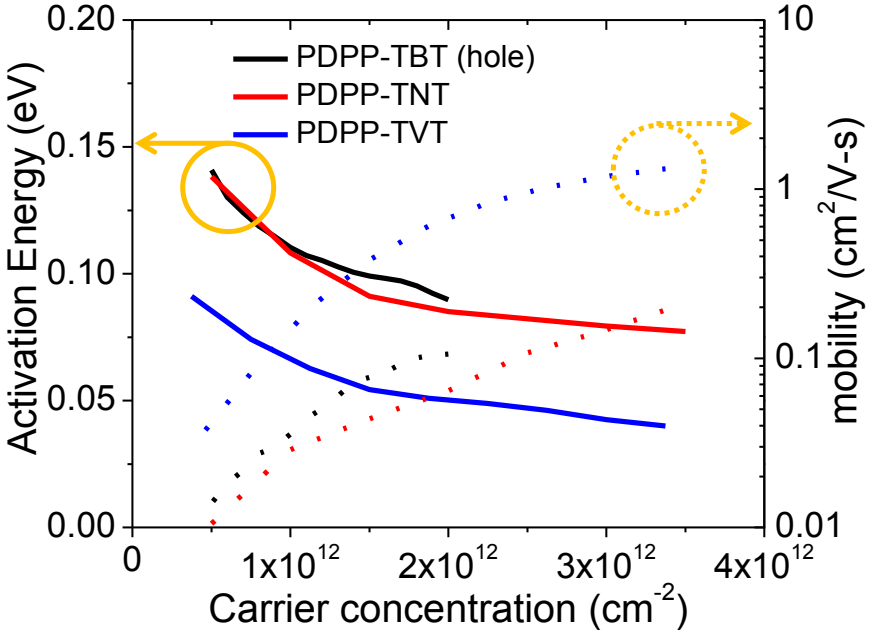


Figure 5.13 The plot of the activation energy and mobility as a function of carrier concentration with different DPP-based materials

Figure 5.14 (a) shows normalized transient drain current response in top-, bottom- and dual-gate operations. The normalized transient responses in dual-gate operation shift to shorter "turn-on time" than in single-gate operation, as shown in Figure 5.14 (a). The decrease in "turn-on time" in dual-gate mode means that effective mobilities become higher compared to single-gate mode. Furthermore, the time to reach quasi equilibrium in dual-gate operation is less than in single-gate operation. The corresponding velocity distribution of charge carriers in dual-gate operation shifts to higher velocities than in single-gate operation. It is also noted that dual-gate operation exhibits fewer low velocity carriers compared to single-gate operation. The results support that the dual-gate configuration influences the charge carrier transport and velocity distributions. In dual-gate devices the charges move, on average, further away from the insulator interface. This will impact the extent of trapping and be reflected in the velocity distribution.

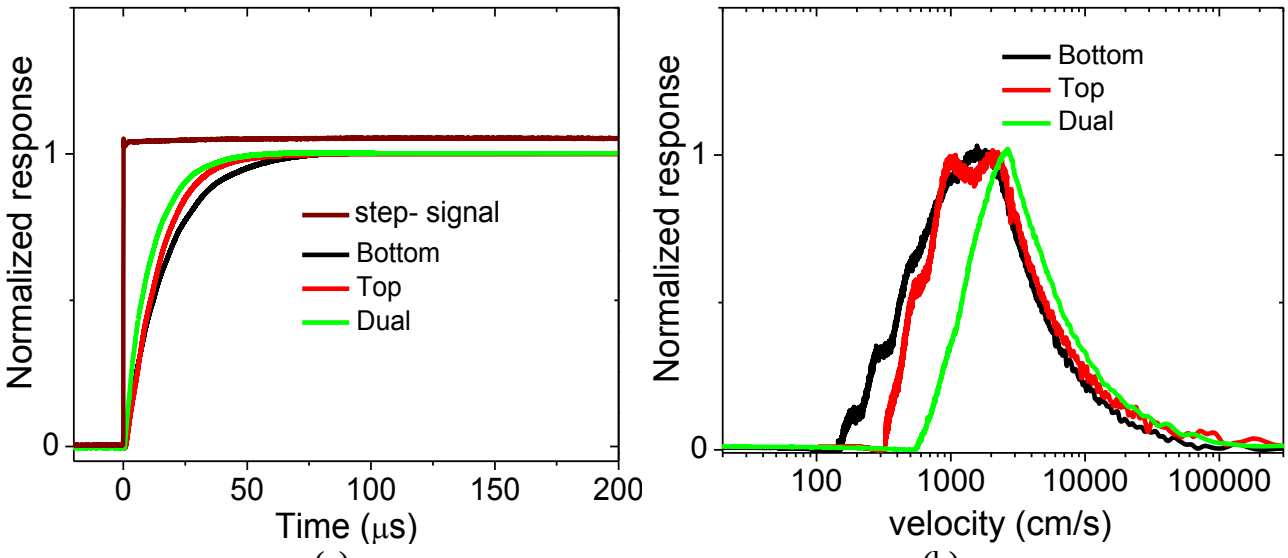


Figure 5.14 (a) normalized transient response and (b) corresponding velocity distributions of charge carriers in top-, bottom- and dual-gate operation

5.5 Conclusions

We have fabricated PDPP-TVT FETs employing dual-gate and 4-point-probe configurations which exhibit room temperature field-effect mobilities of up to 2.6 cm^2/V-s with low electrical contact resistance. We have also investigated the effect of solvents and post-annealing temperatures on PDPP-TVT semiconductors based TFTs with AFM images and electrical characteristics. Charge transport in PDPP-TVT TFTs was discussed using steady-state and under NQS measurements. The observation of clear Arrhenius behavior together with a decrease in activation energy with increasing V_{GS}-V_{ON} indicate that the main charge transport in this polymer semiconductor can be explained by an MTR or Monroe model. In addition, we have compared the activation energies for charge transport in the top-gate and bottom-gate configurations. The activation energy measured under top-gate operation is less than that under bottom-gate operation, which means that corresponding energy distance from occupied trap states to the transport level in top-gate operation is shallower than bottom-gate operation. Comparison of mobilities and activation energies of PDPP-TVT with those of other polymers such as regioregular poly(3-hexylthiophene) (P3HT), poly[5,5'-bis(3-alkyl-2-thienyl)-2,2'-bithiophene] (PQT), and poly[2,5-bis(3-alkylthiophen-2-yl)thieno(3,2-b)thiophene) (PBTTT) indicate that the electronic overlap and intrinsic mobility are higher for this polymer.

CHAPTER 6 TRANSFORMATION OF THE ELECTRICAL CHARACTERISTICS OF GRAPHENE FIELD-EFFECT TRANSISTORS WITH FLUOROPOLYMERS AND ORGANIC SEMICONDUCTORS

6.1 Introduction

Electronic devices with an active channel consisting of a single layer graphene have been of great scientific and technological interest due to its high carrier mobility and stable mechanical and chemical properties [38-44]. In particular, very fast charge carrier transport combined with mechanical and thermodynamic stability can be key enablers to promising nano-scale and sub-millimeter wave electronic devices applications [52, 154-157]. Graphene based FETs have been shown to operate at very high frequencies [55, 158-159]. However, since a single layer graphene has no bandgap in principle, the current in graphene FETs is difficult to turn off completely by gate bias compared to silicon-based devices, which limits the possible use of such transistors in digital circuits [53-54]. For many electronic circuit applications it will be desirable to improve the on-off current ratio so that graphene resembles a semiconductor more than a semimetal.

Research and manufacturing of organic semiconductors has been developing rapidly during the past few decades. Most of the studies on graphene in organic devices have focused on its metallic conductivity for use as an electrode [160-161]. It must be noted that there have been no studies on FETs with hybrid graphene/organic semiconductor active layers. In this chapter, we describe the electrical characteristics of hybrid graphene/organic semiconductor FETs employing α-sexithiophene (α–6T) and

hexadecafluorocopperphthallocyanine ($F_{16}CuPc$) for the organic materials. We also demonstrate a general method to favorably transform the electrical characteristics of graphene FETs by capping with fluoropolymers such as CYTOP®. Key metrics such as mobility, on-off current ratio and residual carrier density, n_o, are all improved. We present a hypothesis as to why this alteration happens.

6.2 Chemical-vapor-deposited mono-layered graphene

As a first step, good quality mono-layered graphene films were synthesized on 500 nm thick e-beam evaporated copper films grown on a Si/SiO_2 substrates, by the low-pressure chemical vapor deposition (LPCVD) as described below [162-163]. The samples were first annealed for 5 minutes at 1000 ºC in a hydrogen-containing ambient. The hydrogen gas was purged away at the end of the annealing process and ultra-high purity (99.99%) methane was circulated at a flow rate of 10 sccm for 5 minutes during the growth process. After growth, the chamber was slowly cooled down to below 180 ºC before unloading of samples.

The graphene films were then transferred to a Si/SiO_2 substrate by a conventional wet-transfer process [162-163]. In the wet-transfer process, graphene on copper film was first spin coated with poly(methyl methacrylate) (PMMA) at 4000 rpm for 1 minute. The sample was kept in desicator overnight for removing the solvent (chlorobenzene) in PMMA. It was then placed into Buffer Oxide Etch (6:1) to etch way the SiO_2 to have PMMA-Graphene-Cu film detached from the substrate. It is important to remove the SiO_2 first to have the surface of copper film exposed. Otherwise we have to use strong

solution of copper etchant to etch it from sides and it causes defect in graphene which shows up in the Raman spectrum after transfer. The film was carefully taken out of the Buffer Oxide Etch with a spoon and put in DI water. It was then placed in dilute ammonium persulfate solution (Transene, APS 100) to etch away the copper. After the copper film was completely etched away, the PMMA-Graphene film was rinsed with DI water couple of times. The target substrate was held inside the water in an inclined manner and was positioned just under the film. The substrate was then gently pulled out of the water with the PMMA film on top. After the sample was dried in desicator overnight to remove water, it was heated on hotplate at 120^{o}C for 2 minutes. This step is crucial because it involves some tradeoff. Heating PMMA to higher temperature (usually 180^{o}C, which is above PMMA glass transition temperature-Tg) for longer time causes the PMMA to reflow and film adhesion to the substrate to be better. However, this also causes the PMMA to stick to graphene and it gets difficult to remove it later in acetone without appropriate annealing condition. This is why the sample was heated just above PMMA Tg for a short time. PMMA was then removed in acetone. The acetone was replaced with fresh supply twice over the span of 24 hours. Finally the sample was rinsed in IPA and dried in air.

Figure 6.1 shows Raman spectra on CVD grown mono-layered graphene. The full width at half maximum (FWHM) of the 2D-peak is ~29 cm^{-1} [164-165]. The intensity ratio between 2D and G peaks is 2.8. The D peak (defect related peak) intensity is small or negligible. AFM images of the graphene show a polycrystalline film, as shown in

Figure 6.1. These results indicate that the mono-layered graphene in the FET is of high material quality.

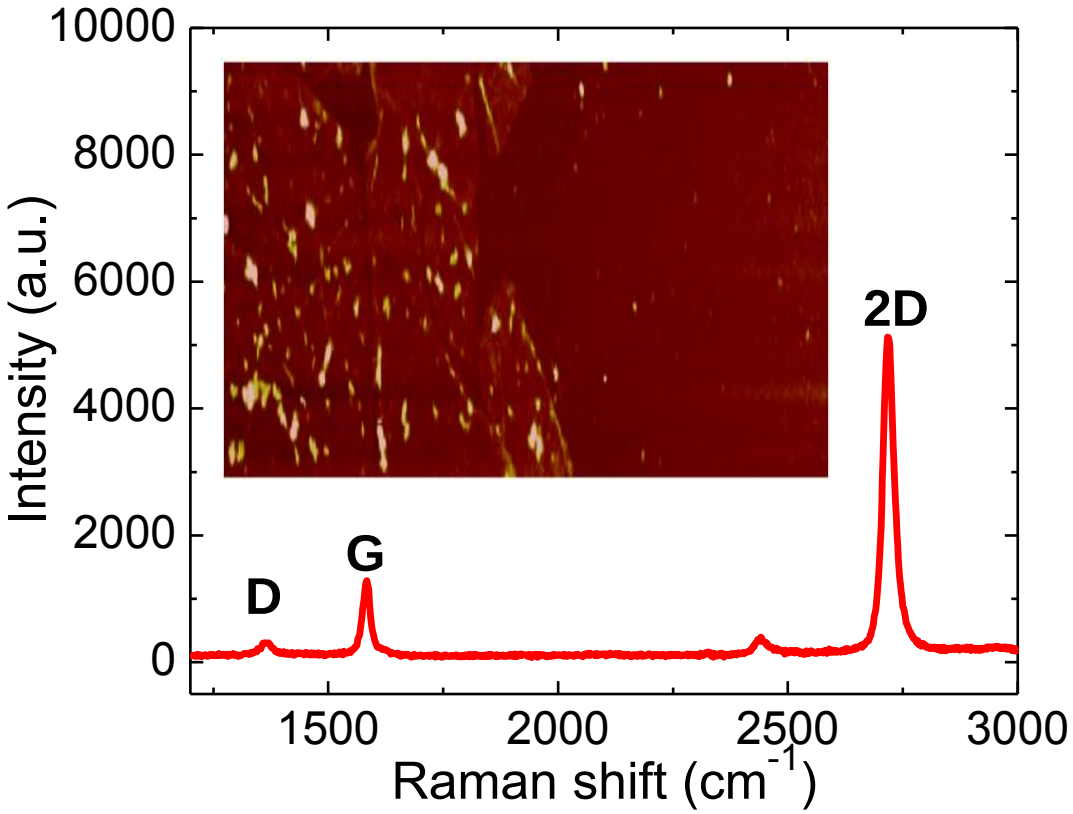


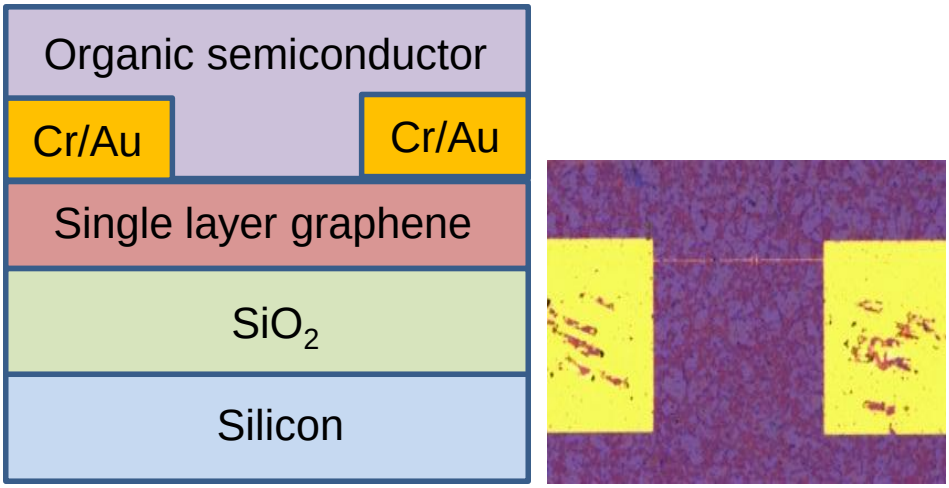
Figure 6.1 Raman spectra on CVD grown mono-layered graphene with a 442 nm blue laser. The inset shows AFM image of CVD grown mono-layered graphene after graphene transfer

6.3 Hybrid graphene/organic semiconductor FETs

6.3.1 Experiments

Figure 6.2 (a) and (b) show the schematic cross-section and optical image of a hybrid graphene/organic semiconductor FET. The device fabrication process starts with

1-10 Ω-cm n-doped silicon substrate employed as the bottom-gate electrode. It is thermally oxidized to result in a 290 nm thick silicon dioxide bottom gate insulator. A single layer graphene was synthesized by a LPCVD on a 500 nm thick copper film. Source/drain electrodes were patterned by electron-beam lithography and lift-off and then a chrome/gold (2.5 nm/50 nm) bi-layer was deposited by thermal evaporation. The sample was kept in high vacuum for 2 days to minimize impurity incorporation. A 15nm thick layer of organic semiconductor (either α-6T or F_{16}CuPc) was deposited by thermal sublimation at a rate of 0.1 Å/s under a pressure of 10^{-7} Torr. Substrate heating at 180-200 ºC was applied to improve the quality of semiconductor films. Optimized bottom gate bottom contact α-6T and F_{16}CuPc FETs possess field-effect mobilites of 0.03 and 0.02 cm^2/V-s in air, respectively. These values are consistent with the highest reported mobilities for these materials [166]. In order to remove organic semiconductors from hybrid graphene/organic semiconductor FETs, they were subject to heat treatment using a substrate heater at 250-300 ºC under high vacuum. This causes the organic semiconductor film to sublime away. Hybrid graphene/organic semiconductor FET possesses a channel width of 8 μm and a channel length of 4 μm. DC measurements for the device characteristics were carried out using Agilent 4155C semiconductor parameter analyzer.

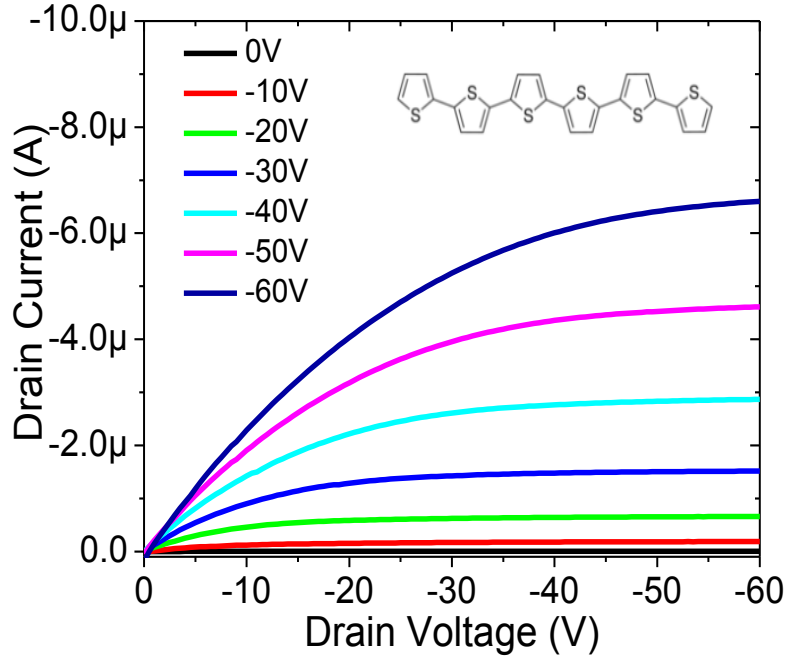


(a) (b)

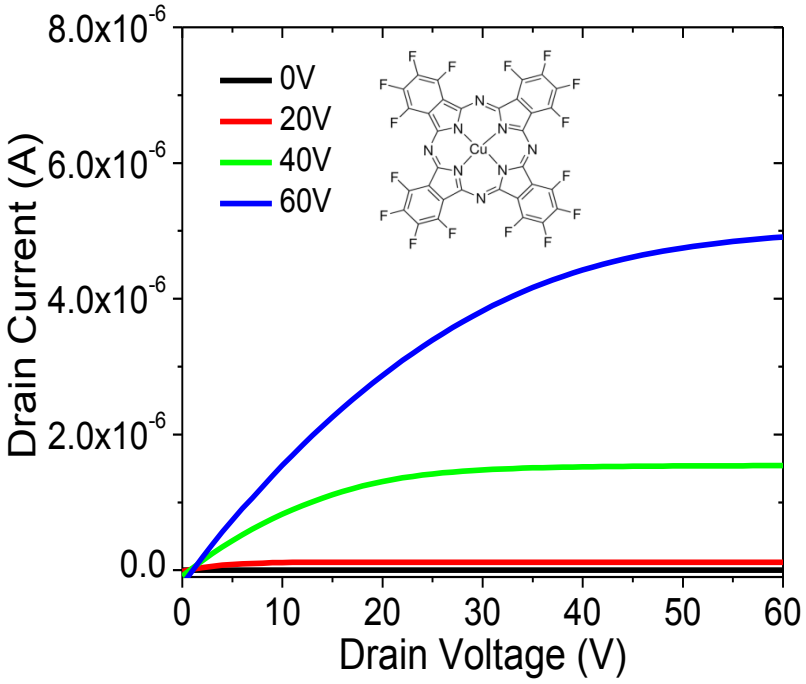
Figure 6.2 (a) schematic cross-section and (b) optical image of a hybrid graphene/organic semiconductor FET

6.3.2 RESULTS

Figure 6.3 (a) and (b) show the output characteristics of optimized bottom-gate bottom-contact α-6T and F_{16}CuPc FETs. α-6T FETs possess hole-dominant transport whereas F_{16}CuPc exhibits electron-dominant transport. In order to improve the quality of π-conjugated organic semiconductor, substrate heating was employed. Good output characteristics were observed with low electrical contact resistance. The extracted field-effect mobilities from α-6T and F_{16}CuPc FETs are 0.03 cm^2/V-s and 0.02 cm^2/V-s, respectively.



(a)



(b)

Figure 6.3 (a) The output characteristics of optimized bottom-gate bottom-contact α-6T and F_{16}CuPc FETs

Figure 6.4 (a) shows the transfer characteristics of a hybrid graphene/organic semiconductor FET employing α-6T semiconductor at the drain-source voltage of 0.1 V during the sweep of gate voltage from -70 V to 70 V. The transfer characteristics of a graphene FET are not degraded by depositing organic semiconductor onto the graphene layer. It can be noted that the transfer characteristics of hybrid graphene/organic semiconductor FETs return to its initial state (i.e., before organic semiconductor deposition) after removing α-6T semiconductor layer. The electronic properties of graphene can be tuned favorably using the capping layer of organic semiconductor.

In order to extract the key parameters, a diffusive transport model based on total resistance of the graphene device was used [167].

$$R_{TOTAL} = R_{CONTACT} + \frac{L}{We\mu\sqrt{n_o^2 + n[V_G{}^*]^2}}$$

Where μ is the field-effect mobility, $n[V_G^*]$ is the value of the carrier concentration induced by the gate bias away from the Dirac point and no is the density of carriers at the minimum conductivity point. Figure 6.4 (b) shows there is good agreement between the experimental data and diffusive transport model. Optimized graphene/organic semiconductor FETs with α-6T possess field-effect mobility of 1289 cm^2/V-s in air, which is slightly improved from 1176 cm^2/V-s in single layer graphene FET without a decrease in the on-off current ratio. The extracted no is 10^{12} cm^{-2} and width-normalized contact resistance is ~1.9 kΩ-μm. Furthermore, removal of the organic semiconductor layer from graphene FETs results in a return to the original electronic properties. The

results suggest that there are weak reversible electronic interactions between organic semiconductor and graphene layers.

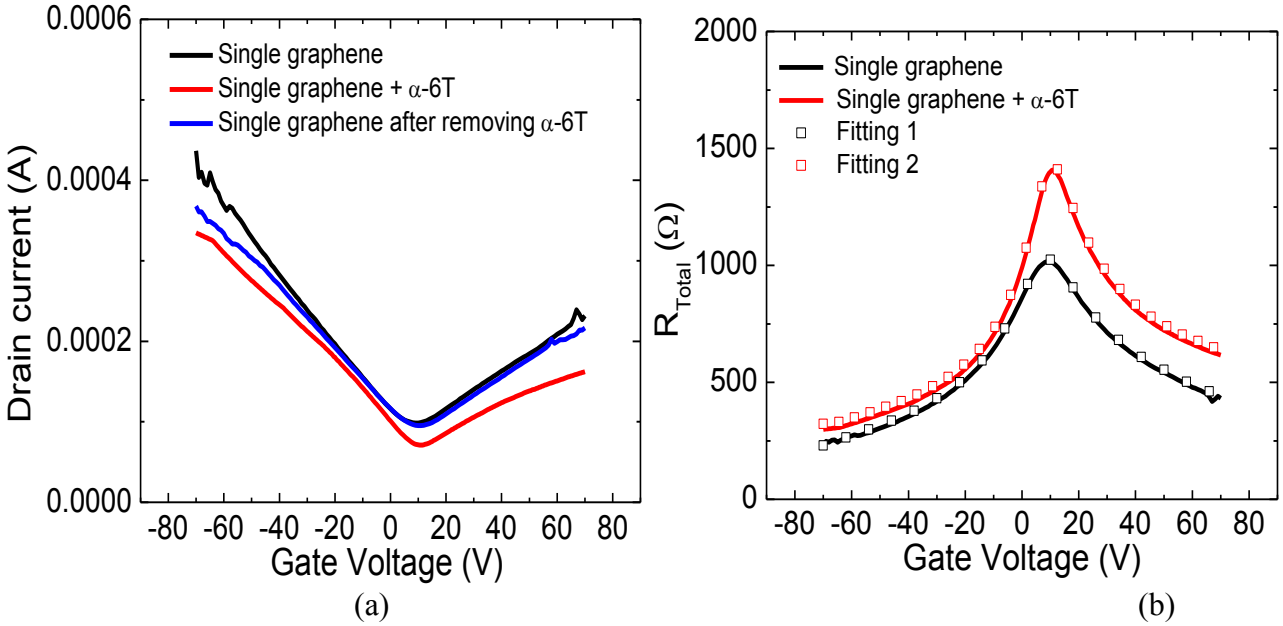


Figure 6.4 (a) The transfer characteristics of single layer graphene, graphene by capping with α-6T and graphene FETs after removing α-6T at the drain-source voltage of 0.1V during the sweep of gate bias from -70V to 70V. The inset shows the chemical structure of α-6T and (b) the total resistance along with diffusive transport modeling fit

The on-off current ratio and the field-effect mobility in a graphene FET are typically decreased after depositing most additional layers on grapheme [158]. Figure 6.5 shows the transfer characteristics and the normalized resistance of single layer graphene by capping with α-6T semiconductor layer and with silicon dioxide. Compared to silicon dioxide on a graphene FET, the on-state current ratio in graphene/ α-6T FET was improved from 3 to 5 and on-current was increased by factor of two without degradation in field-effect mobility. It means that weak interaction between α-6T semiconductor and

graphene influences the electronic characteristics including charge carrier transport, which is obviously distinguished from silicon dioxide. The nature of this interaction is elucidated later in this chapter.

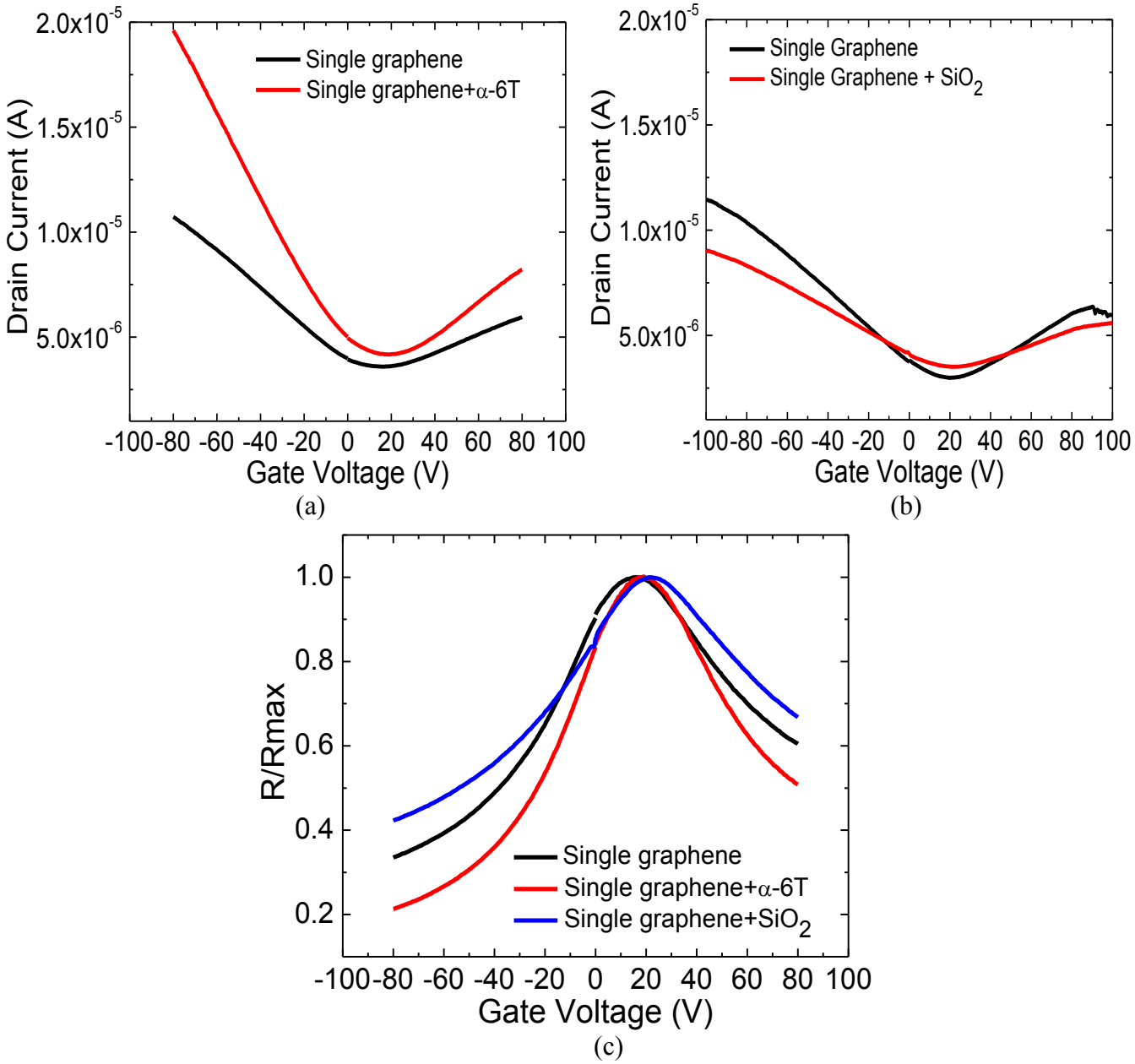


Figure 6.5 (a) The transfer characteristics of single layer graphene by capping with (a) α-6T and (b) silicon dioxide. (c) the normalized resistance in single layer graphene and graphene FETs by capping with α-6T and silicon dioxide

It has been reported that fluorination of graphene can dramatically alter its electronic and optical properties, affording orders of magnitude increase in the resistivity and opening of a bandgap of several eV [168]. The effect of capping with $F_{16}CuPc$ on graphene FETs was investigated, as shown in Figure 6.6. Compared to the plain single layer graphene FET, capping with $F_{16}CuPc$ improved on-off current ratio from 3 to 5 as well as the field-effect mobility from 1292 to 1367 $cm^2/V\text{-}s$ in air. Furthermore, the Dirac voltage point was shifted to a more negative voltage. The value of the extracted no is decreased from $1.3x10^{12}$ to $1.0x10^{12}cm^{-2}$, indicating that a significant favorable modification of electronic properties occurs with the introduction of the fluorinated semiconductor.

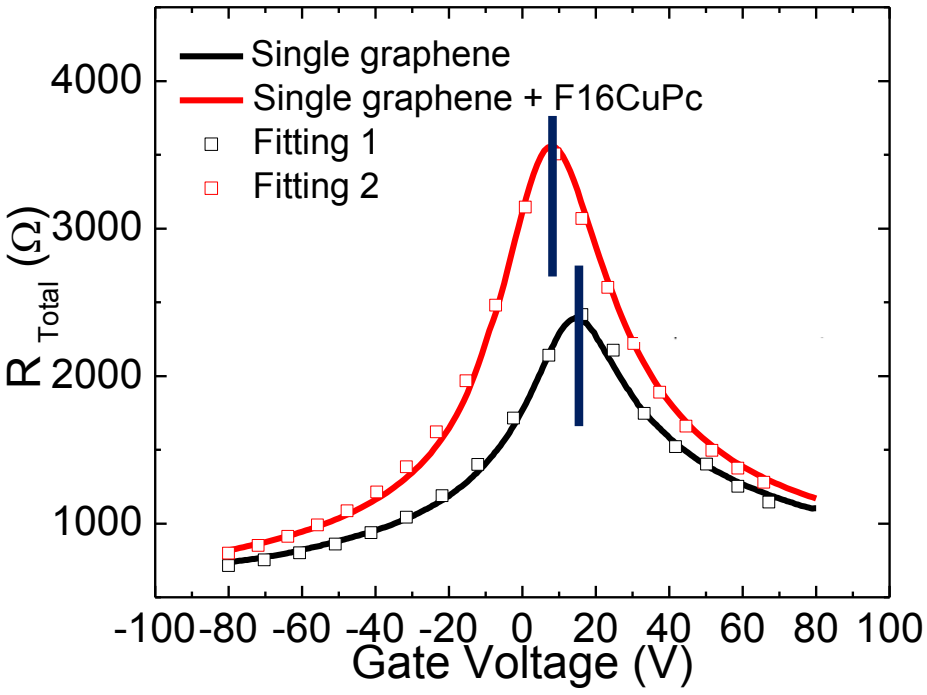


Figure 6.6 (a) The total resistance in single layer graphene and graphene FETs by capping with $F_{16}CuPc$ along with diffusive transport modeling fit The inset shows the chemical structure of $F_{16}CuPc$

6.4 Transformation of the electrical characteristics of graphene FETs with fluoropolymer

For many electronic circuit applications it will be desirable to improve the on-off current ratio so that graphene resembles a semiconductor more than a semimetal. In achieving such a transformation, the high mobility must not be reduced and preferably increased. We demonstrate another method to favorably transform the electrical characteristics of graphene FETs by capping with fluoropolymers such as CYTOP® and Teflon-AF®. With this approach we get even better results compared to that obtained with organic semiconductors described in the last section. The conductivity at the Dirac point is reduced and the mobility is increased, leading to an improvement in the on-off current ratio to ~ 10, the highest that has been hitherto achieved in graphene. Remarkably, all key graphene device metrics are improved including electron-hole transport symmetry, Dirac voltage, and reduced impurity doping. We note that, in general, attempts to coat graphene with inorganic dielectrics such as silicon dioxide and aluminum oxide have not resulted in an improvement in electrical characteristics. Importantly, these results have been achieved in graphene grown by wafer-scale CVD process. From a practical standpoint, this is a significant advance in that it offers a clear path to improve the performance characteristics of graphene FETs in which the active material is grown by wafer-scale CVD. CVD graphene is the most promising method of realizing large area graphene and in adapting graphene for silicon CMOS and flexible electronics [169]. The improved mobilities and reduced conductivities will open up the range of applications for graphene circuitry.

6.4.1 EXPERIMENTS

Figure 6.7. shows the illustration of fabrication process flow of a mono-layered graphene FET after capping with the fluoropolymer. Good quality mono-layered graphene films were formed as described in section 6.2. Oxygen plasma reactive-ion-etching (RIE) was used to pattern the active channel region, to remove the superfluous graphene and to ensure device isolation. Source/drain electrodes were patterned by electron-beam lithography and lift-off. The titanium/gold (2.0 nm/50 nm) bi-layers that form the source/drain contacts were deposited by thermal evaporation under high vacuum. Deposition of good quality titanium and gold in high vacuum conditions (~10^{-7} torr) are key to realizing low-resistance electrical contacts. The samples were kept in high vacuum for 2 days to minimize impurity incorporation. Mono-layered graphene FETs fabricated as described above feature possess a channel width of 5 μm and a channel length of 1 μm.

A 90 nm thick layer of the fluoropolymer, CYTOP® (Asahi Glass Co.) was deposited by spin-coating a diluted CYTOP® solution (CYTOP®: solvent = 1: 10) on mono-layered graphene and annealed gradually from 30 ºC to 180 ºC for over a span of 1 hour in a nitrogen atmosphere. A 140 nm thick layer of Teflon-AF® (Dupont Co.) was also spin-coated with as-supplied Teflon-AF® solution on mono-layered graphene. The samples were annealed gradually from 30 ºC to 300 ºC for over a span of 1 hour in a nitrogen atmosphere. In order to remove the CYTOP® from graphene FETs, the samples were immersed in a CYTOP® solvent for 24 hours. This removes most of the CYTOP®.

The temperature-dependent measurements were performed in a Desert Cyrogenics vacuum probe station with a chamber pressure lower than 10^{-3} Torr. DC measurements for the device characteristics were carried out using Agilent 4155C semiconductor parameter analyzer.

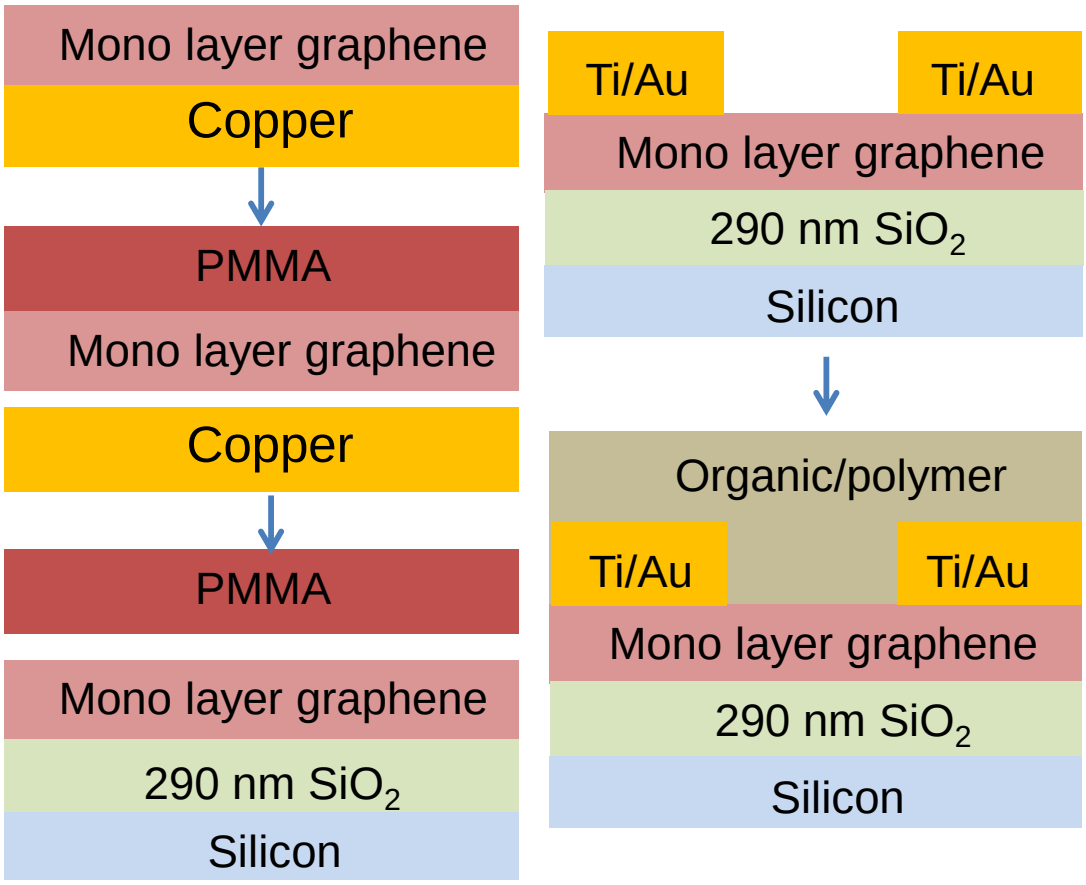
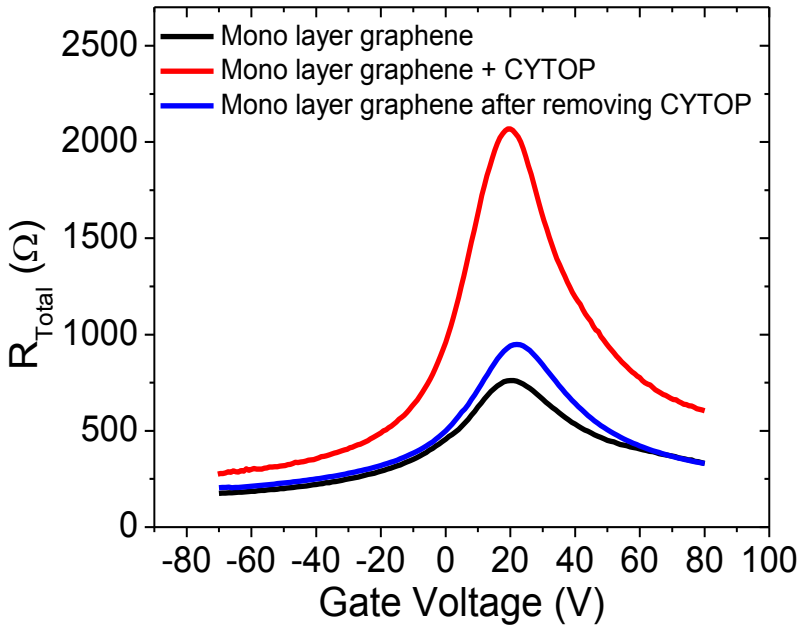


Figure 6.7 Illustration of fabrication process flow of a mono-layered graphene FET after capping with the fluoropolymer

6.4.2 Results

Figure 6.8 (a) shows the transfer characteristics of as-deposited mono-layered graphene FET without capping with CYTOP®, with capping with CYTOP®, and after removal of CYTOP®. The drain-source voltage is 0.1 V during the sweep of the gate voltage from -70 V to 80 V. It is generally observed that device characteristics such as on-state current, field-effect mobility and on-off current ratio in graphene FETs are reduced after the deposition of most dielectrics materials on graphene due to charge scattering [170-172]. It is observed that in the present case, the off-state current (at the Dirac point) is decreased substantially, resulting in a net improvement in the on-off current ratio with the use of CYTOP®. This is illustrated more clearly in Figure 6.8 (b) which shows that the on-off current ratio is improved from 5 to 10 after depositing CYTOP® on graphene FETs. In addition, the field-effect mobility was improved from 1731 to 3606 cm^2/V-s, width-normalized contact resistance is not appreciably altered from ~ 400Ω-μm and residual carrier density n_o is reduced. The results indicate that electrical device characteristics of graphene FETs are significantly improved through the interaction between fluoropolymer and mono-layered graphene, which is different from the interaction of graphene with most dielectrics such as silicon dioxide, aluminum oxide and hafnium oxide [171-172]. When the CYTOP® layer was removed by using CYTOP® solvent from mono-layered graphene FETs, the transfer characteristic tends to return to its initial state (i.e. that of mono-layered graphene before CYTOP® deposition), as shown in Figure 6.8 (a). These results mean that the interaction between graphene and CYTOP® is weak enough to permit easy removal of CYTOP® [173-174] .



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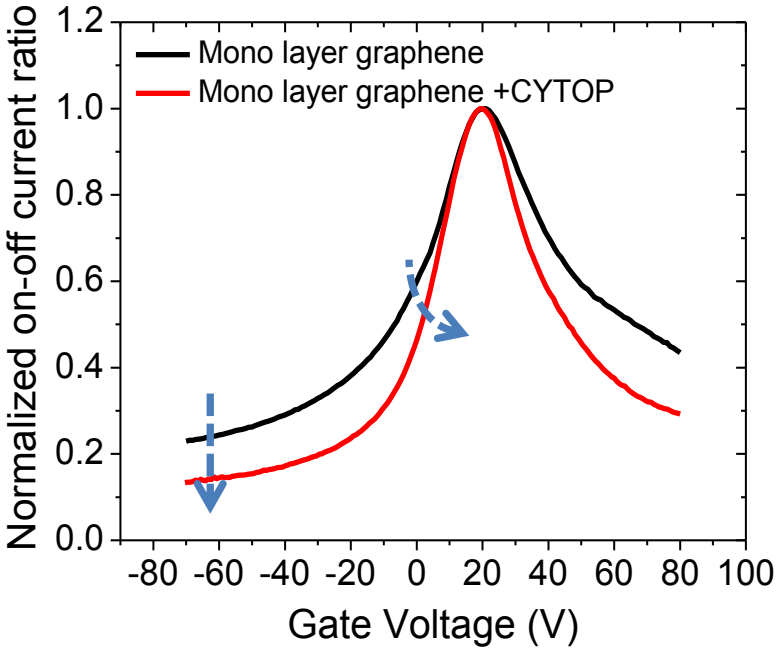


(b)

Figure 6.8 (a) The transfer characteristics of mono-layered graphene, graphene with CYTOP® capping layer and graphene FETs after removing CYTOP® .The drain-source voltage is 0.1V and (b) Improvement in the normalized on-off current ratio after depositing CYTOP® on mono-layered graphene FET.

Raman spectra were measured with a 442 nm blue laser on mono-layered graphene capped with CYTOP®. Figure 6.9 shows the change in the Raman spectrum of mono-layered graphene produced by the capping layer of CYTOP®. The intensity of the D band at 1350 cm^{-1} was strongly increased after capping the graphene with CYTOP®. At the same time, the intensity of the 2D band at 2700 cm^{-1} and the G band at 1580 cm^{-1} were slightly decreased. Significantly, a new low-intensity band at 2940 cm^{-1} was observed on mono-layered graphene FETs with CYTOP®, which is not observed before depositing CYTOP®. Appearance of this new band in the Raman spectrum was previously reported in fluorinated graphene [174-176].

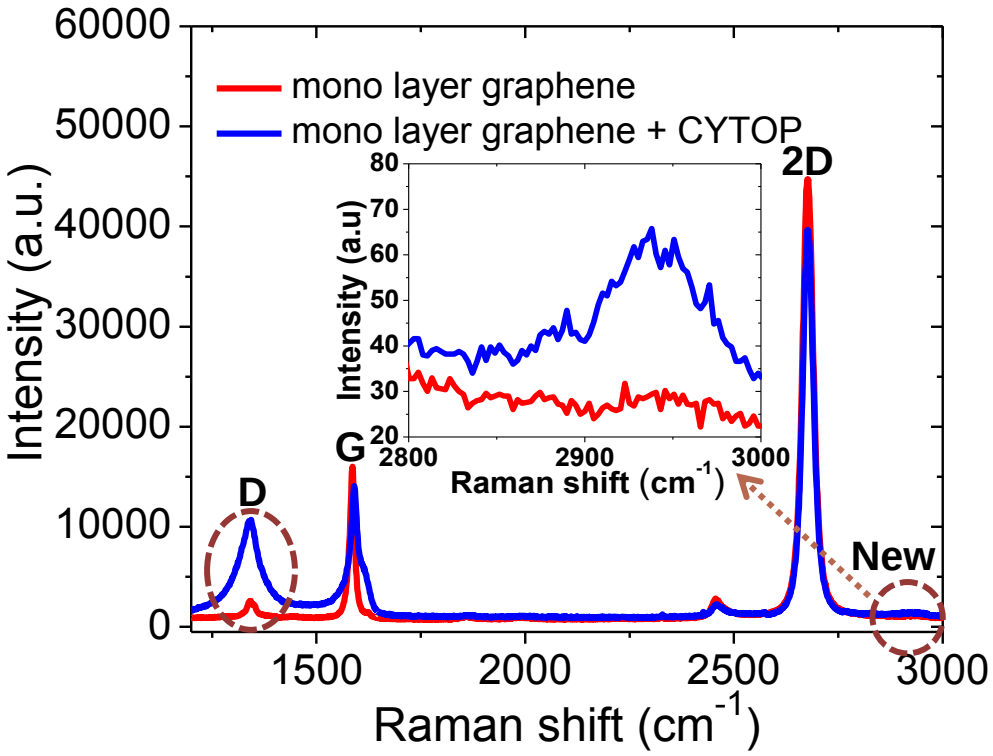


Figure 6.9 Change in Raman spectrum measured with a 442 nm blue laser of mono-layered graphene with and without CYTOP® capping layer

The C-F bonds in the CYTOP® structure are very polar and graphene is a highly polarizable material [177-179]. The electronic interaction between the dipoles in the CYTOP® and the graphene can modify its electronic properties significantly, leading to the effects that we observe. We note that with non-polar organic capping layers such as pentacene, no significant changes in the electrical properties of graphene FETs are observed as shown in Figure 6.10.

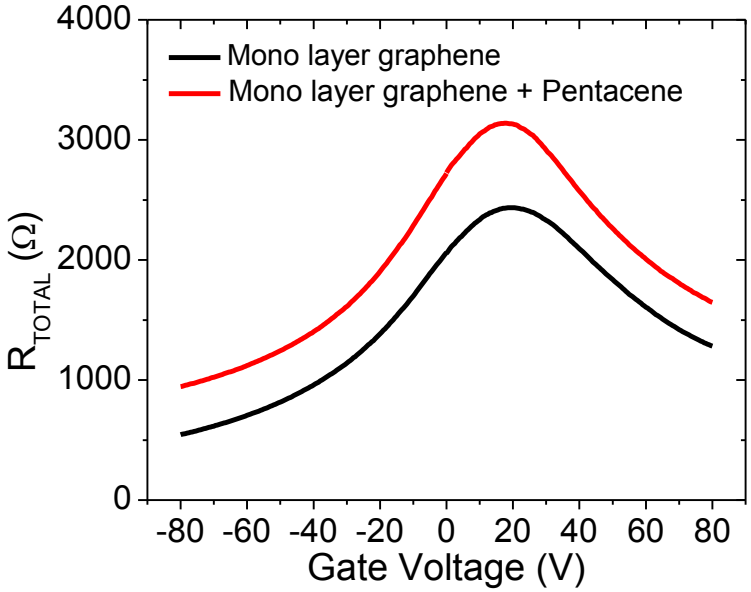
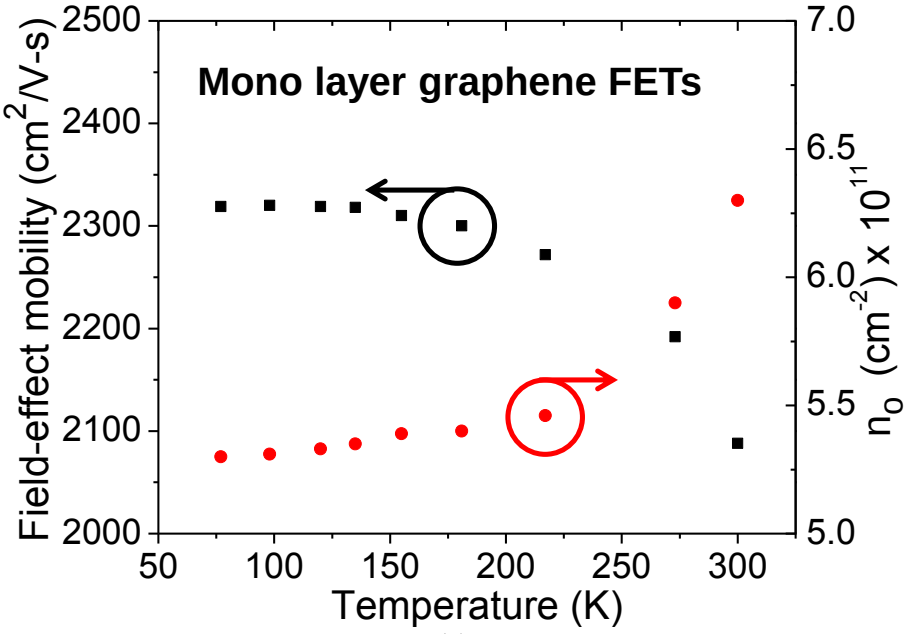


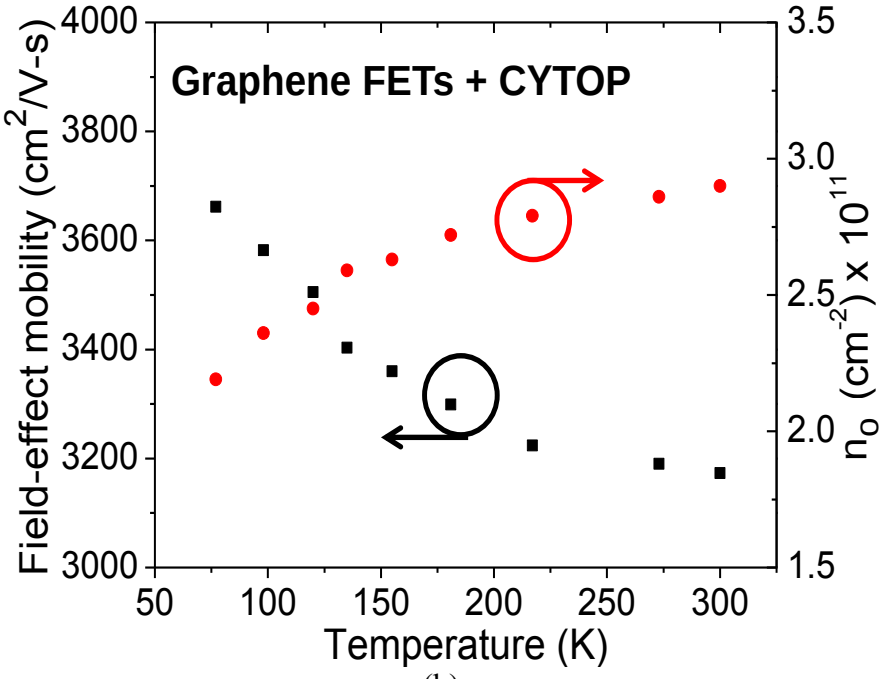
Figure 6.10 The total resistance of mono layer graphene with and without capping with Pentacene. There is no significant change in the on-off current ratio.

We have verified our hypothesis in the case of a second fluoropolymer, Teflon-AF® possessing polar C-F bonds, which also results in a marked improvement in electrical properties of graphene upon capping. The origin of this improvement is in the strongly polar nature of the C-F chemical bond found in the capping materials we have employed

together with the tendency of these materials to self-organize upon heat treatment such that there is an oriented layer of dipolar C-F bonds at the interface with graphene. We believe that this dipole layer results in a reduction of the dimensionless fine structure constant (α) [180]. A reduction in fine structure constant improves the mobility which is limited by long-range scattering by charged impurities while simultaneously, the minimum conductivity, determined by short-range scattering, decreases [180]. This results in an improved on-off ratio, which has so far been a problem for graphene FETs. Temperature dependent mobility and impurity studies also show that with capping, the impurity scattering limited mobility continues to increase with reducing temperature which is accompanied by a reduction in n_0 as shown in Figure 6.11. The CYTOP® dipoles could also break the symmetry between the A and B sub-lattices in graphene, leading to the development of a small energy gap, which is also consistent with our results [181-183].



(a)



(b)

Figure 6.11 (a) Temperature dependent mobility and no in (a) mono-layered graphene FETs vs. (b) graphene FETs capped with CYTOP®: Studies show that with capping, the impurity scattering limited mobility continues to increase with reducing temperature which is accompanied by a reduction in n_o

The effect of capping with CYTOP® on doped mono-layered graphene FETs is shown in Figure 6.12. The on-off current ratio was improved from 6 to 9 as well as the field-effect mobility was increased from 1753 to 3045 cm^2/V-s without change in width-normalized contact resistance after depositing CYTOP®. In addition, the residual carrier density no is reduced from 1.03×10^{12} to 5.2×10^{11} cm^{-2}. Significantly, there is a large shift in the Dirac voltage point. The fluorocarbon capping method is therefore a way to restore or greatly improve the properties of graphene that are otherwise non-ideal. These effects are accompanied by a favorable shift in the Dirac voltage toward zero. In some cases of Teflon-AF®, this shift in Dirac voltage is very dramatic, with shift magnitudes in excess of 60 V, as shown in Figure 6.12.

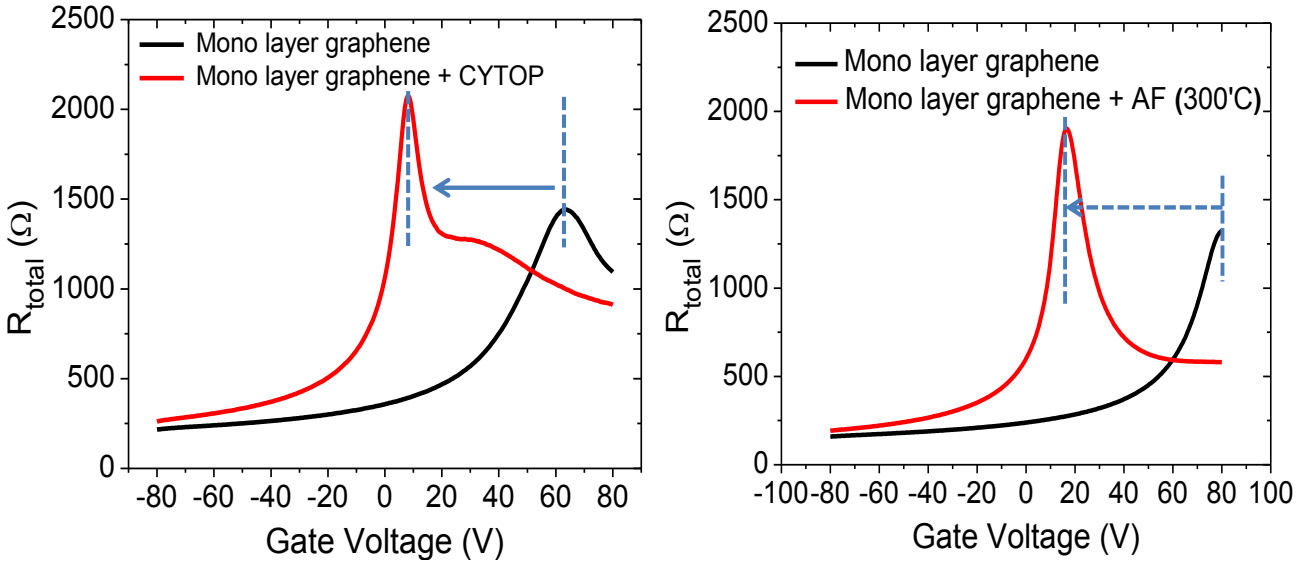


Figure 6.12 Transformation of characteristics of mono-layered graphene by capping with (a) CYTOP® and (b) Teflon-AF® at the drain-source voltage of 0.1V during the sweep of gate bias from -80V to 80V. The substantial shift in the Dirac voltage toward zero after depositing CYTOP® and Teflon-AF® can be noted.

The capping materials that we have chosen all possess C-F bonds and processing conditions have been employed that results in the materials ordering in a manner that results in a strong net dipole moment at the interface with graphene. Additional experiment and theoretical work is being done to understand these effects in more detail and will be reported elsewhere. The fact that the strength of this interaction is dependent on the annealing temperature of the CYTOP® and Teflon-AF® also suggests that annealing improves the ordering of the fluoropolymer and consequently the total dipole strength. In the case of the two fluoropolymers post-deposition annealing (at temperatures up to 300^{o}C) was employed to enable material reorganization and the side chain alignment that is commonly observed in these materials. For the organic semiconductor, F_{16}CuPc, material deposition was performed at elevated temperatures (up to 200^{o}C). Previous work has shown that such elevated deposition temperatures results in the best ordered materials resulting in relatively high mobility in these semiconducting films [166].

It can be clearly observed as shown in Figure 6.13 that the electrical properties of CYTOP-coated graphene steadily improve with annealing temperature (in the range 60-180^{o}C) demonstrating that the side-chain alignment that accompanies such annealing is a key factor in the transformation of electrical properties. It is noteworthy that if the CYTOP® is removed after the annealing, then the original graphene characteristics are recovered indicating reversible non-covalent interactions.

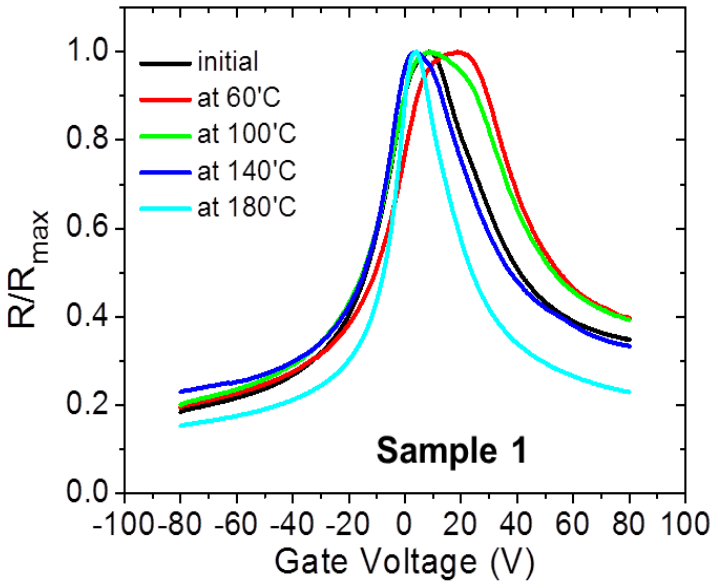


Figure 6.13 The electrical properties of CYTOP-coated graphene FETs with annealing temperatures

While many of these results can be explained in terms of a modification of the fine structure constant, we note that graphene is very polarizable and changes to the electronic structure and, consequently transport properties, can result from having oriented dipoles to top of the graphene. Additionally, we have modified the electronic environment on only one side of the graphene mono-layered. If both interfaces have highly polar bonds juxtaposed, then the favorable effects we report can be further enhanced.

6.5 Conclusions

In summary, we have investigated hybrid graphene/organic semiconductor FETs with α-6T and F_{16}CuPc. The electronic properties of graphene based FETs can be

favorably tuned by capping with π-conjugated organic semiconductor molecules, particularly F_{16}CuPc. The off-state current was reduced while the on-state current and mobility were either unaffected or increased. We have also shown that the electrical characteristics of graphene are favorably altered by capping with the fluoropolymer CYTOP® and Teflon-AF®. The on-off current ratio is improved and the Dirac voltage shifted toward zero. The residual carrier density n_o is reduced and the mobility increased by as much as a factor of two. We hypothesize that this alteration in electrical properties is a result of electronic polarization of the graphene by local C-F bonds or other dipoles in the fluoropolymer or semiconductor. The strength of this interaction is dependent on the annealing temperature, which influences the ordering of the polymer and consequently the local dipole field. The approach we described offers a way to transform the electrical characteristics of graphene making it potentially more useful for a wider range of electronic applications.

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